



Constructive Boolean Networks and the Exactness of (Timed) Ternary Simulation

Michael Mendler

[joint work with Tom Shiple, Gérard Berry;
Formal Methods in System Design, Vol. 40, No. 3, June 2012]



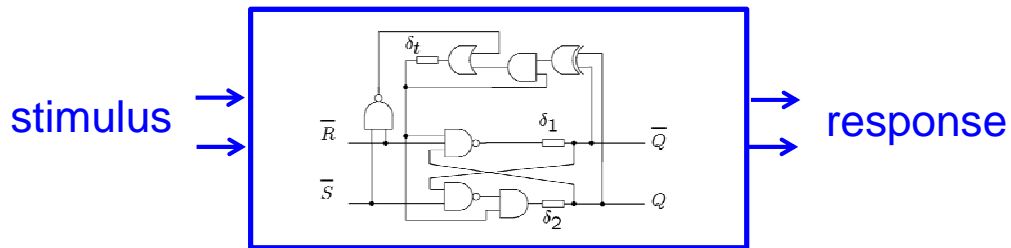
What's this talk about ?

- formally characterise the class of Boolean networks known, informally, as „**constructive**“ **systems** (Berry, Shiple)
- present **correspondence theorems** linking **denotational**, **operational** and **axiomatic** semantics
- highlight that there are **different notions of „causal“** or **„combinational“** systems depending on the MoCC (model of coordination and communication)



COMBINATIONAL NETWORKS

Combinational Networks

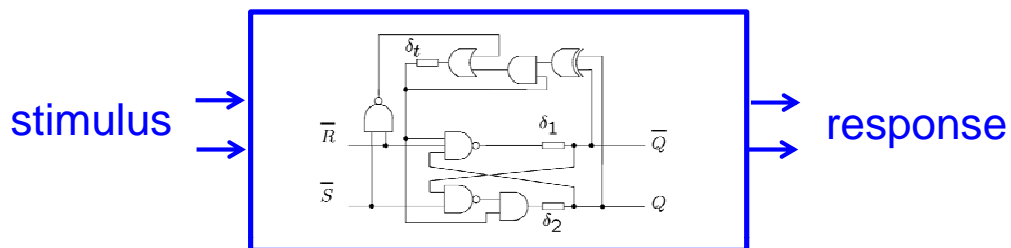


Definition (informal)

A Boolean network (circuit + delay nodes) is **combinational** if it realises a **functional relationship** input \rightarrow output.

- Asynchronous Circuits
- Synchronous Programming (e.g., Esterel, Lustre, ...)
- Communicating Mealy machines (e.g., Statecharts)

Combinational Networks



Definition (operational)

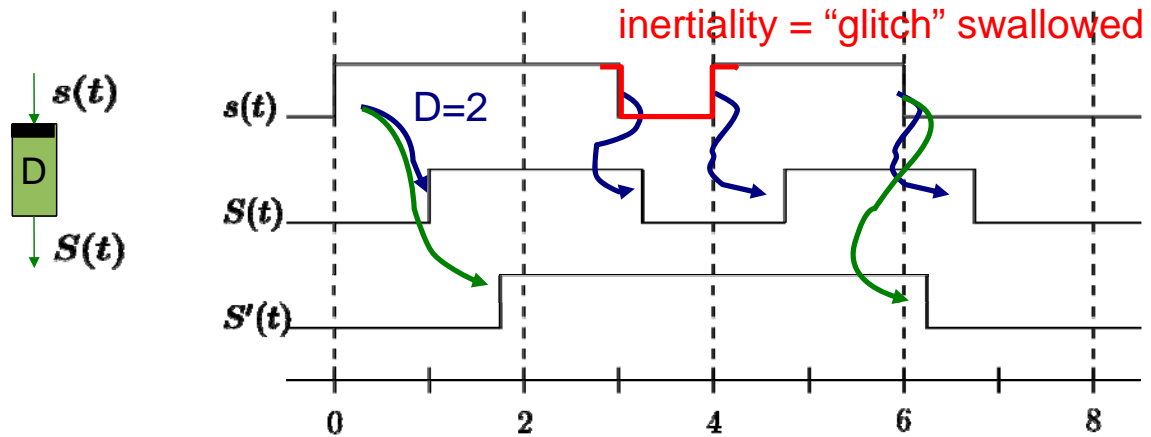
Let **DEL** be a network **delay/scheduling model** (MoCC).

A network is **DEL-combinational** if for all constant input signals every output node

- **stabilizes** in **bounded time**
 - to a **unique response** value
- under DEL-execution semantics.

Up-bounded Inertial Delay (UIN)

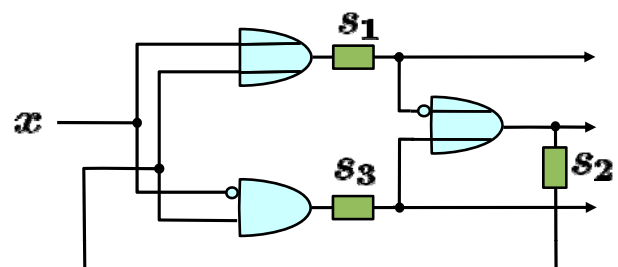
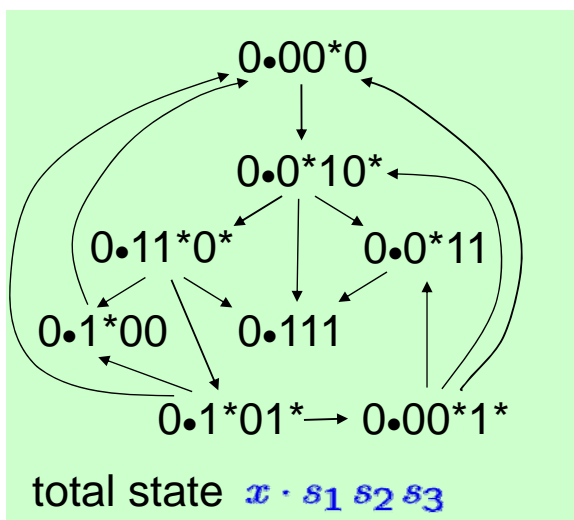
[Huffman'54, Miller'65, Brzozowski/Seeger'89]



- (1) **Up-bounded Propagation:** The delay cannot remain unstable for longer than D time without changing output
- (2) **Inertiality:** The output only changes if delay is unstable

Example I

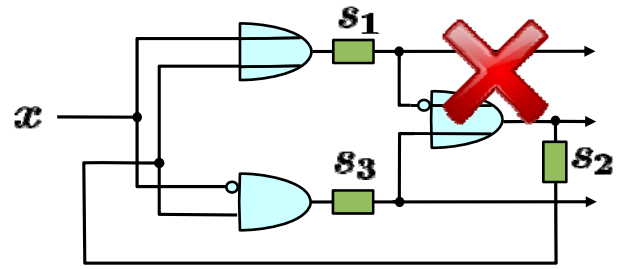
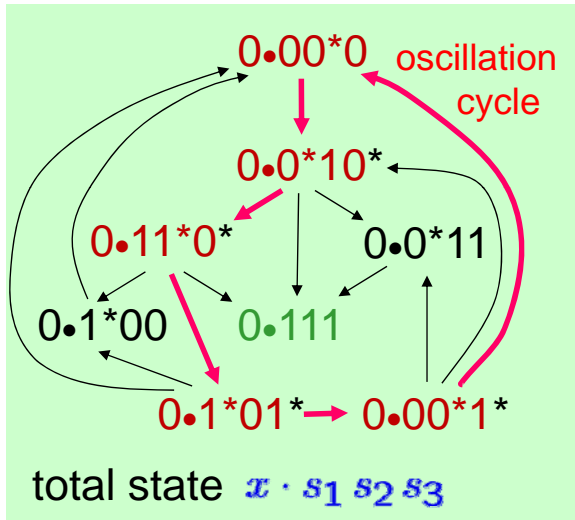
- **Muller Diagram** [Muller'56]
UIN system trajectories



- **Up-bounded Inertial Delay (UIN)**
- **General Multiple Winner Model (GMW)**
[Huffman'54, Brzozowski/Yoeli 79]

Example I

- Muller Diagram [Muller'56]
UIN system trajectories

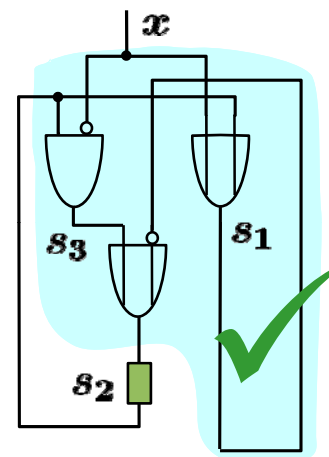
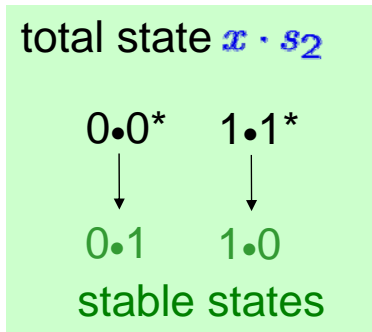


not UIN-combinational !

- Up-bounded Inertial Delay (UIN)
- General Multiple Winner Model (GMW)
[Huffman'54, Brzozowski/Yoeli 79]

Example II

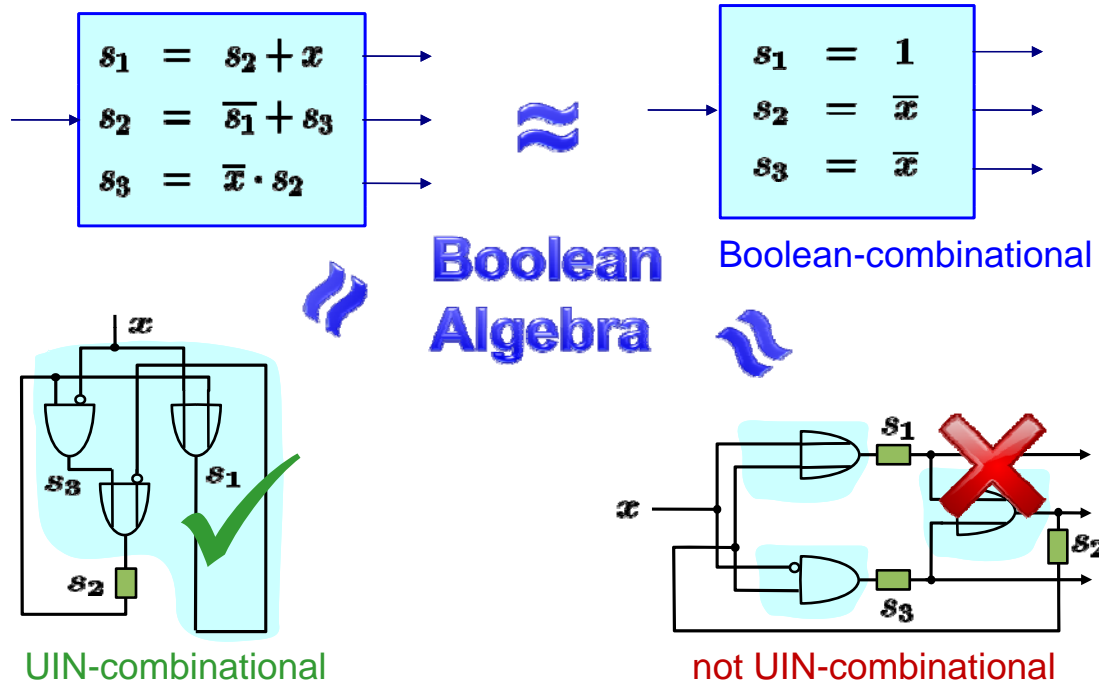
- Muller Diagram
UIN system trajectories



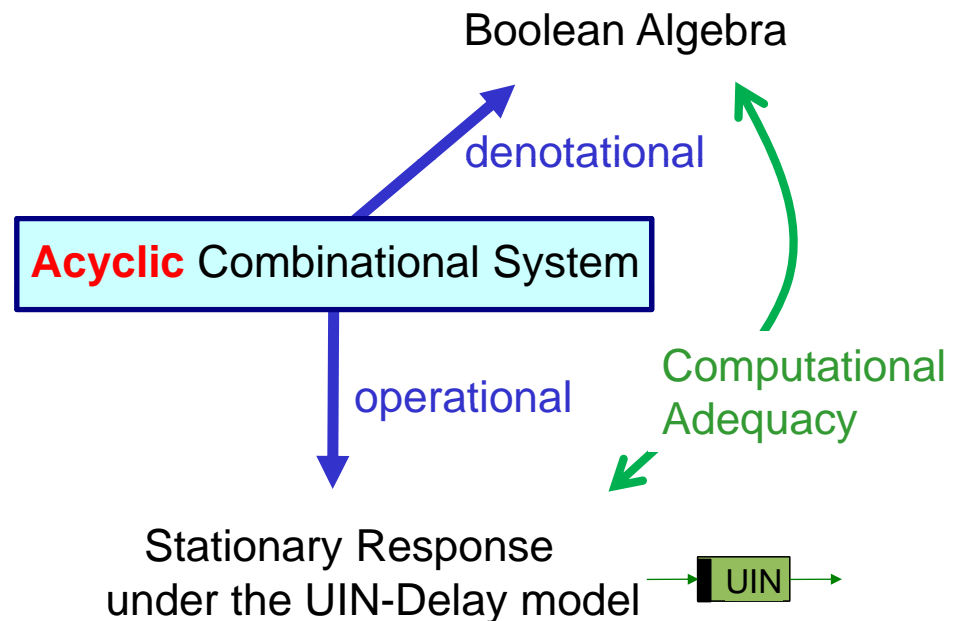
UIN-combinational

- All possible UIN-trajectories in the General Multiple Winner (GMW) model converge !

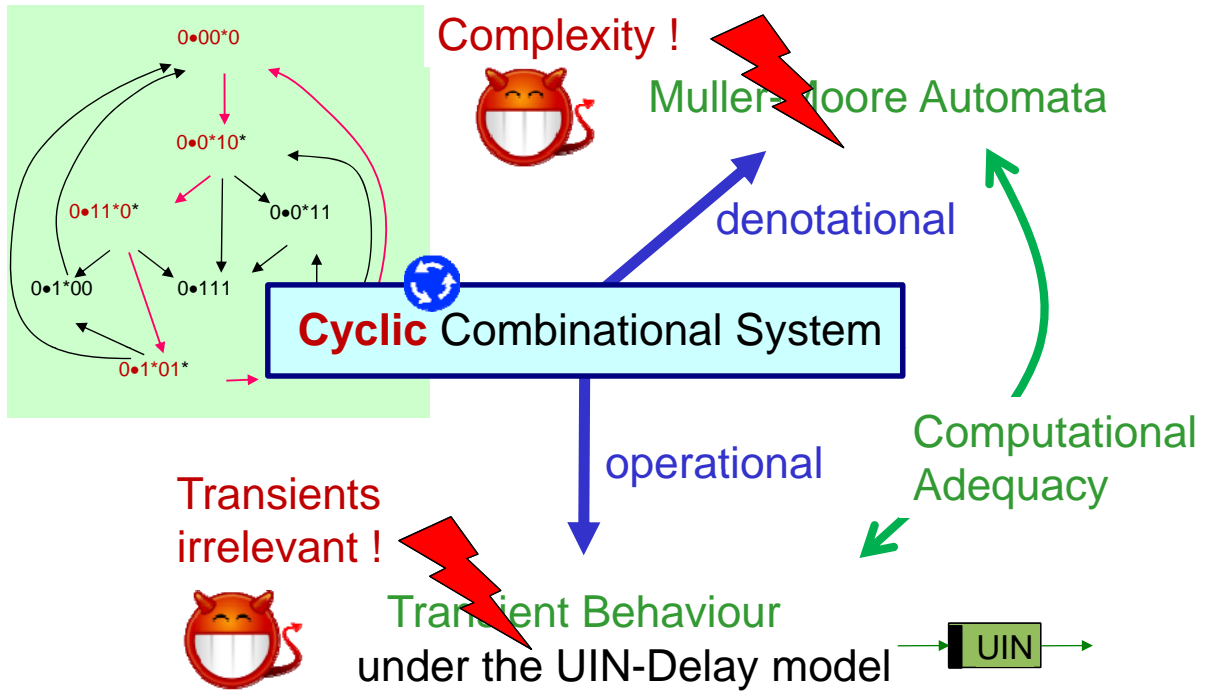
Boolean Paradise Lost



The 2-valued "Steady State Paradise"

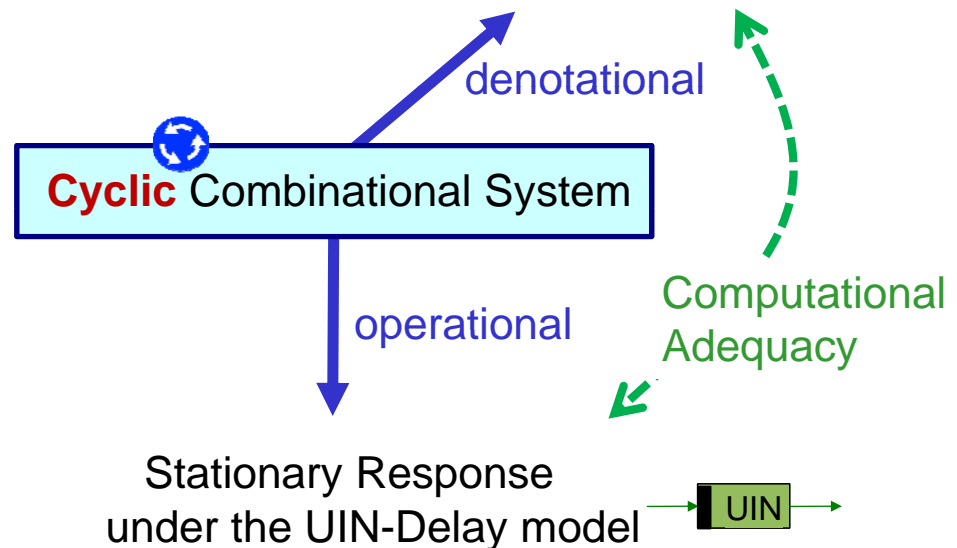


Cycles: "Paradise lost ?"



Cycles: "Paradise lost ?"

What does the engineer do when 2 Booleans are not enough ? ...

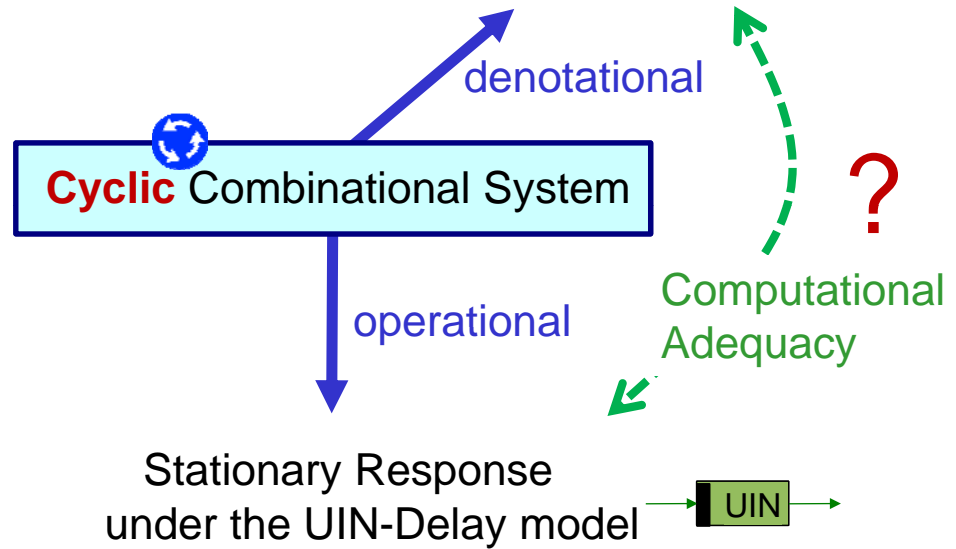




Cycles: "Paradise lost ?"

She asks Kleene to give her a third one ...

Ternary Algebra



TIMED TERNARY SIMULATION

Timed Ternary Algebra

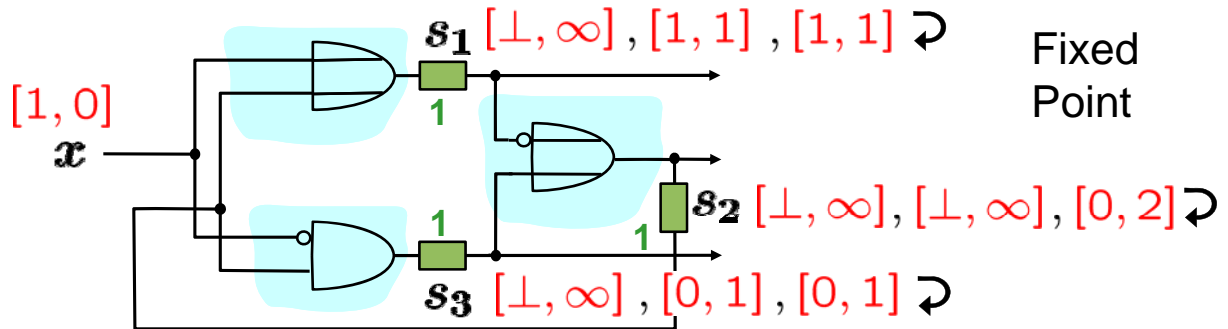
- Recursion theory [Kleene'52]
- Asynchronous Circuits (hazards, races, oscillation)
 - [Yoeli/Rinon'64, Eichelberger'65, Roth'66]
 - [Bryant'87] CMOS transistor-level
- Ternary simulation [Yoeli/Brzozowski'77, Brzozowski/Seeger'95]
- Cyclic combinational circuits
 - [Burch/et.al.'93, Malik'93, Shiple'96]
 - [Huang/Parng/Shyu'91] Timed D-calculus
 - [Fairtlough/Mendler'96] Real-time interpretation
 - [Namjoshi/Kurshan'99, Backes/Fett /Riedel'08] Refined algorithm
- Synchronous programming [Berry'99, Schneider/Brandt/Schuele'04]



Timed Ternary Algebra

	DEL(d)	$\frac{[\alpha, s]}{\perp} \mid \frac{[\alpha, s + d]}{\perp}$		NOT	$\frac{[\alpha, s]}{\perp} \mid \frac{[\bar{\alpha}, s]}{\perp}$
	OR	$\frac{[0, s] \quad [0, t]}{[0, \max(s, t)]}$ $\frac{[1, s] \quad [1, t]}{[1, \min(s, t)]}$ $\frac{\perp \quad \perp}{\perp}$		AND	$\frac{[0, s] \quad [0, t]}{[0, \min(s, t)]}$ $\frac{[1, s] \quad [1, t]}{[1, \max(s, t)]}$ $\frac{\perp \quad \perp}{\perp}$

Example I

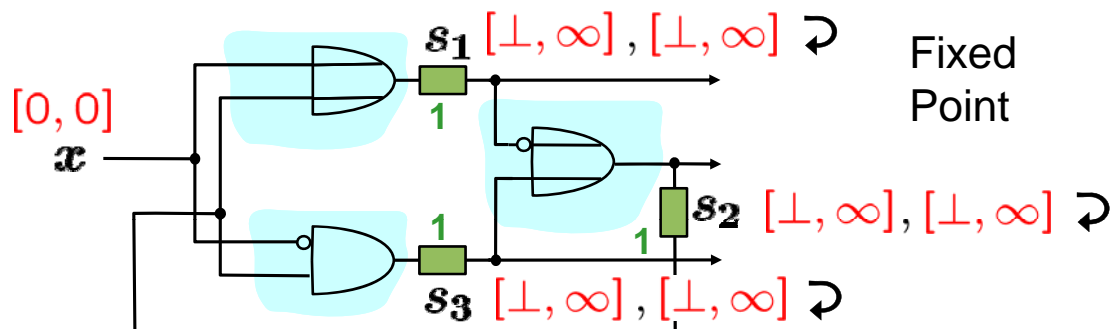


$$s_1^{i+1} = [\text{let } s_2 = s_2^i \text{ in } s_2 + x, 1]$$

$$s_2^{i+1} = [\text{let } (s_1, s_3) = (s_1^i, s_3^i) \text{ in } \overline{s_1} + s_3, 1]$$

$$s_3^{i+1} = [\text{let } s_2 = s_2^i \text{ in } \overline{x} \cdot s_2, 1]$$

Example I



$$s_1^{i+1} = [\text{let } s_2 = s_2^i \text{ in } s_2 + x, 1]$$

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$$s_3^{i+1} = [\text{let } s_2 = s_2^i \text{ in } \overline{x} \cdot s_2, 1]$$

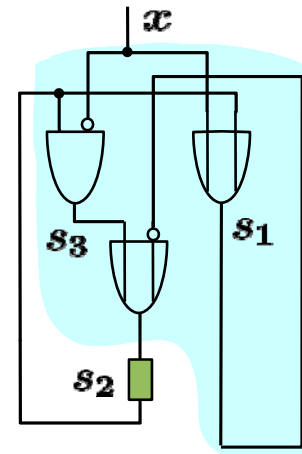
Example II

$$x = [0, 0]$$

$$s_2 = [\perp, \infty], [1, 1] \curvearrowright$$

$$x = [1, 0]$$

$$s_2 = [\perp, \infty], [0, 1] \curvearrowright$$



$$s_2^{i+1} = [\text{let } s_2 = s_2^i \text{ in } \overline{(s_2 + x)} + (\bar{x} \cdot s_2), 1]$$

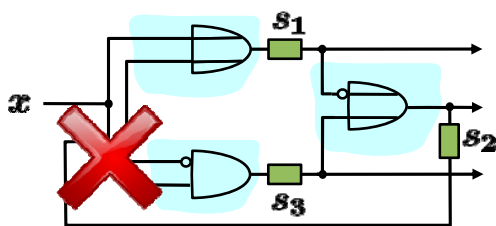
$$= [\text{let } s_2 = s_2^i \text{ in } \bar{x}, 1]$$

$$= [\bar{x}, 1]$$

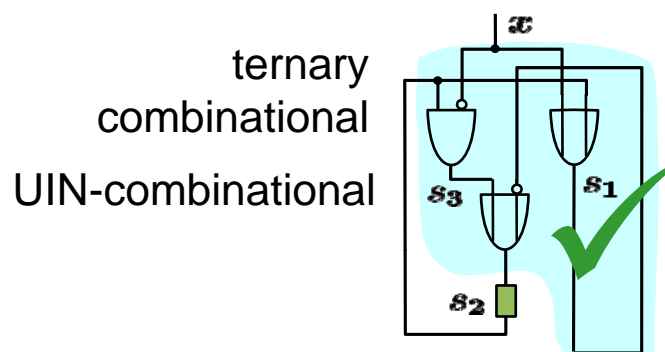
Ternary Combinational Network

Definition

A network (fixed set of state nodes) is **ternary combinational** if the **least fixed point** of its timed ternary extension produces **bounded-time Boolean values** for all (static) input vectors.



not ternary combinational
not UIN-combinational



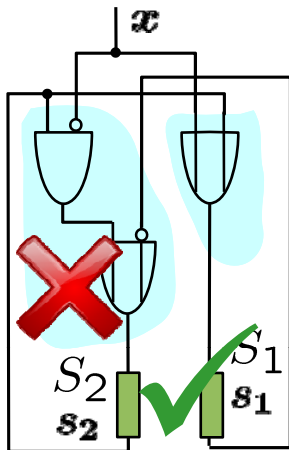


Problem Solved ?



THE ABSTRACTION GAP

UIN-Delay Full Abstraction Problem



$$S_1 = \perp \wedge s_1 = \perp \wedge S_2 = \perp \wedge s_2 = \perp$$

$$S_1 = s_1 \vee S_2 = s_2$$

not ternary comb.

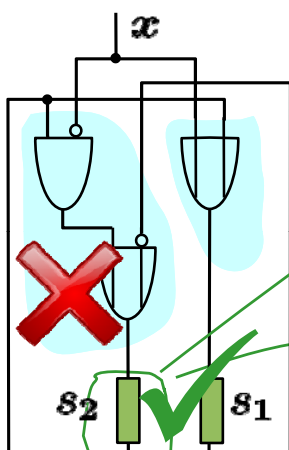
UIN-comb.

?

Ternary simulation too abstract ?

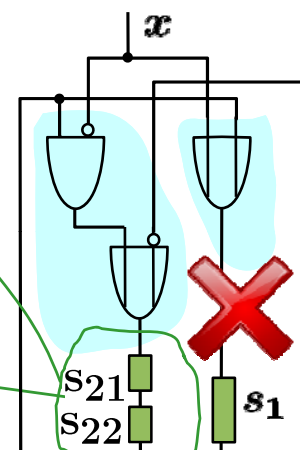
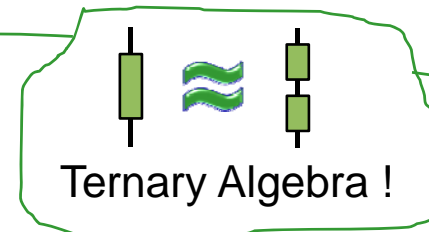
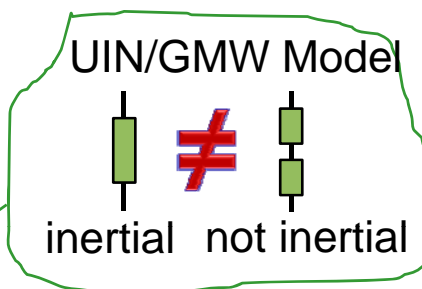
UIN delays too strongly synchronised ?

UIN-Delay Full Abstraction Problem



UIN-comb.

not ternary comb.



not UIN-comb.

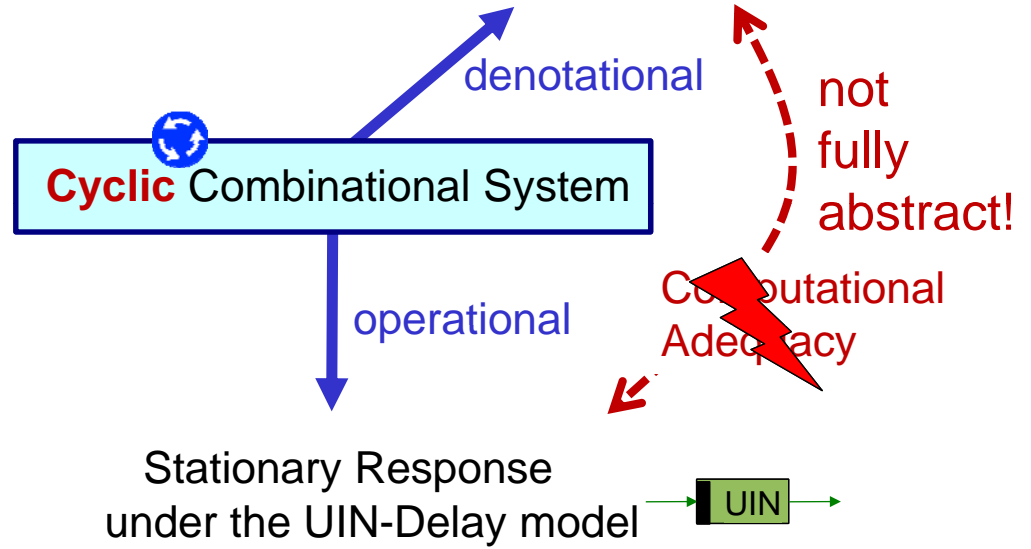
not ternary comb.

- Inertial Delays / GMW are **not quite** the right operational interpretation of Ternary Simulation !



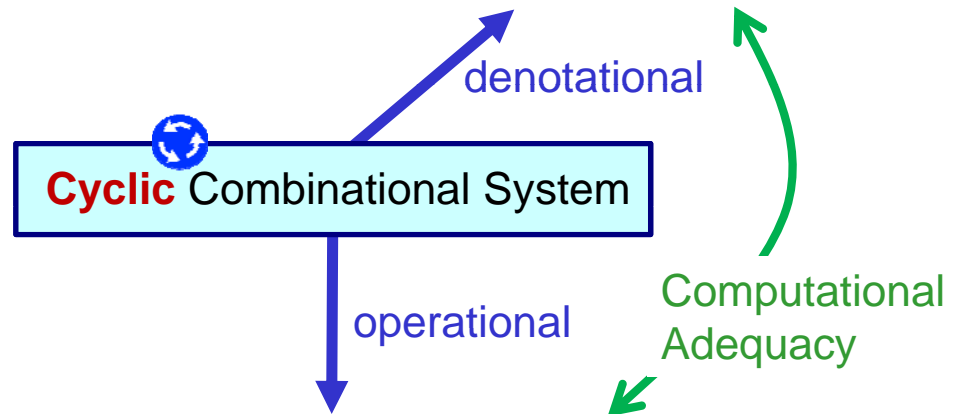
“Paradise lost ?”

Ternary Algebra



“Paradise lost ?”

Ternary Algebra

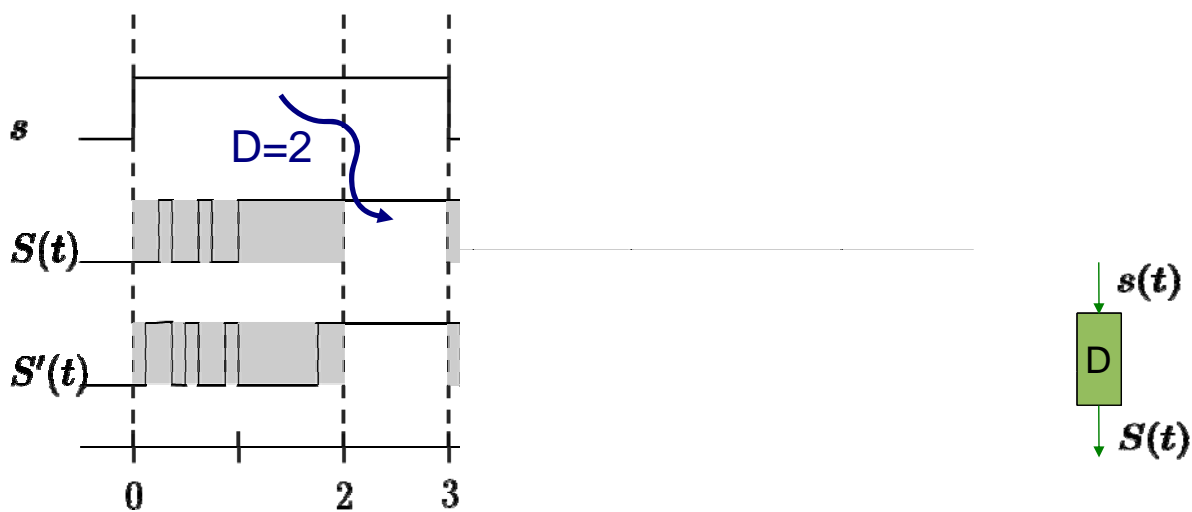


Up-bounded Non-inertial Delays (UNI)

The „right“ operational interpretation of Timed Ternary Simulation:

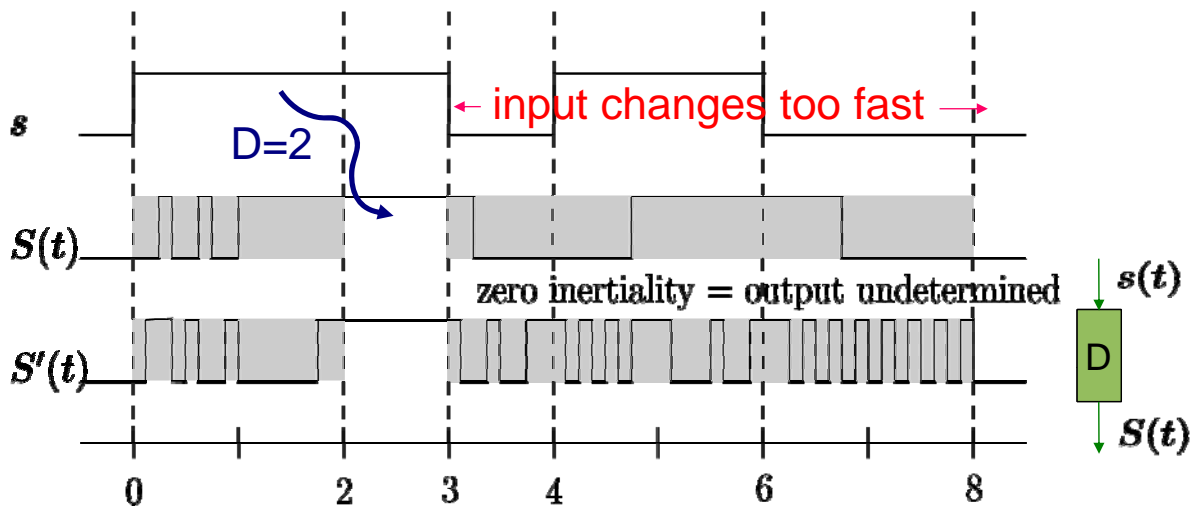
NON-INERTIAL DELAYS

Up-bounded Non-Inertial (UNI-)Delay



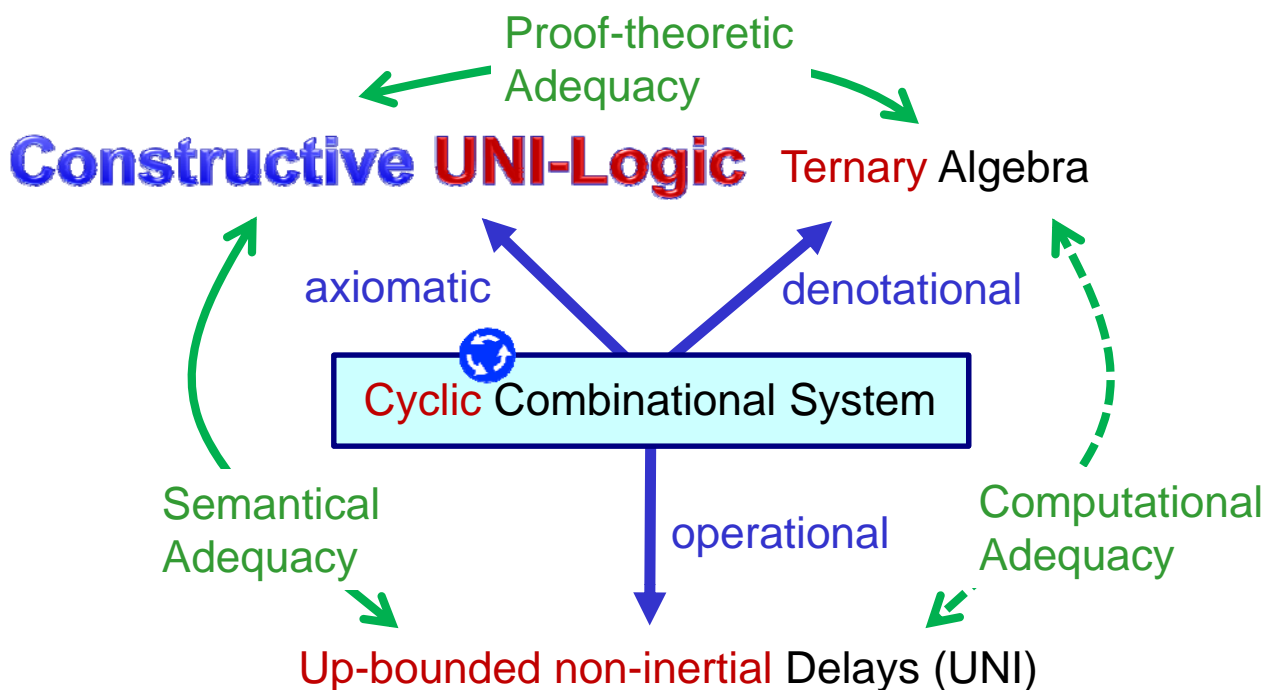
- (1) **Up-bounded Propagation:** If the input remains stable for longer than D time, then the output stabilises to new value.
- (2) **Non-inertial:** If input changes, output totally uncontrolled until new value has propagated through.

Up-bounded Non-Inertial (UNI-)Delay



- (1) **Up-bounded Propagation:** If the input remains stable for longer than D time, then the output stabilises to new value.
- (2) **Non-inertial:** If input changes, output totally uncontrolled until new value has propagated through.

How Do We Prove UNI-Delay Adequacy ?





The „right“ logical interpretation of Timed Ternary Simulation:

CONSTRUCTIVE UNI-LOGIC



Basic Properties

UNI-logic satisfies the **axioms**

$$\phi \supset \diamond_D \phi$$

$$\diamond_D \diamond_E \phi \supset \diamond_{D+E} \phi$$

$$\diamond_D \phi \wedge \diamond_E \psi \supset \diamond_{\max(D,E)} (\phi \wedge \psi)$$

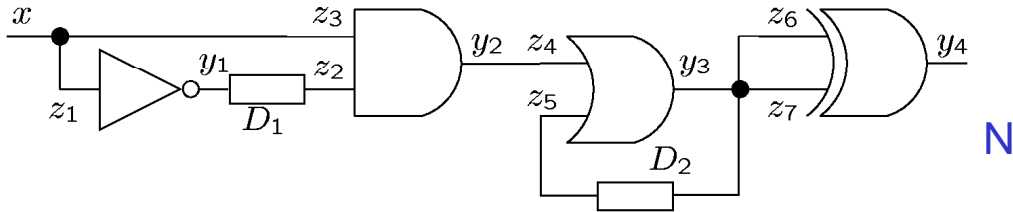
and the **rule** $\models \phi \supset \psi \Rightarrow \models \diamond_D \phi \supset \diamond_D \psi$.

Logic: **lax modality** (pronounced "LAGS")

[Fairtlough & Mendler 97]

Types, Functional Progr.: **strong monads** [Moggi 91]

UN Network Specifications

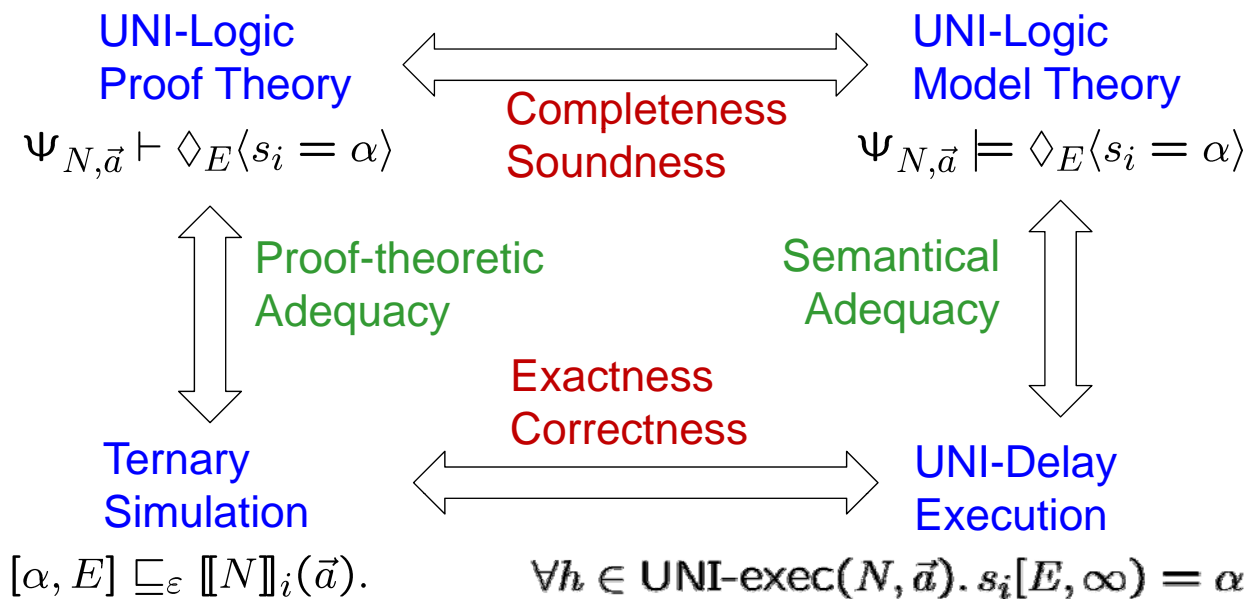


$$\begin{aligned} \Phi_N \equiv & y_1 = \bar{z}_1 \wedge y_2 = z_3 z_2 \wedge y_3 = z_4 + z_5 \wedge \\ & y_4 = z_6 \bar{z}_7 + \bar{z}_6 z_7 \wedge \\ & z_1 = x \wedge z_2 :=_{D_1} y_1 \wedge z_3 = x \wedge z_4 = y_2 \wedge \\ & z_5 :=_{D_2} y_3 \wedge z_6 = y_3 \wedge z_7 = y_3. \end{aligned}$$

$$\phi_1 :=_D \phi_2 \text{ stands for } (\neg\phi_2 \supset \diamond_D \neg\phi_1) \wedge (\phi_2 \supset \diamond_D \phi_1)$$

Lindenbaum/Henkin Construction

For every input \vec{a} and state vertex s_i :



$x = \perp$ „known undefined“ \leftrightarrow „unknown defined“

WHY CONSTRUCTIVENESS MATTERS...

What does constructiveness buy us ?

$\Psi_{N,\vec{a}}$ set of UNI-trajectories of network N and input \vec{a}

Disjunction Property

$\Psi_{N,\vec{a}} \vdash s$ stabilises to 0 \vee s stabilises to 1

$\Rightarrow \Psi_{N,\vec{a}} \vdash s$ stabilises to 0 **or** $\Psi_{N,\vec{a}} \vdash s$ stabilises to 1

Existential Property

$\Psi_{N,\vec{a}} \vdash \exists t. s$ stabilises at time t

\Rightarrow for some **delay bound D**,

$\Psi_{N,\vec{a}} \vdash s$ stabilises at time D

Constructive reaction is always deterministic and bounded !

CONCLUSION

Summary

Theorem — „Constructive Networks“

The following statements are equivalent:

- A network N is provably stable in **UNI-Logic** *axiomatic*
- The **ternary simulation** of N in the chosen state variables generates Boolean solutions *denotational*
- N stabilises in bounded time to a unique steady state under **non-inertial delay** assumptions *operational*



Research Directions

- Expressiveness and Complexity of UNI-Logic ?
- Efficient implementation of timed ternary simulation, symbolically for arbitrary input
- What would be a sound and complete Logic for
 - Up-bounded inertial delays ?
 - bi-bounded delays, transport delays, ...
- Comprehensive classification of combinational circuit hierarchies



Thank you !