Universität Bamberg

Informatics Theory Group
Faculty of Information Systems and Applied Computer Sciences

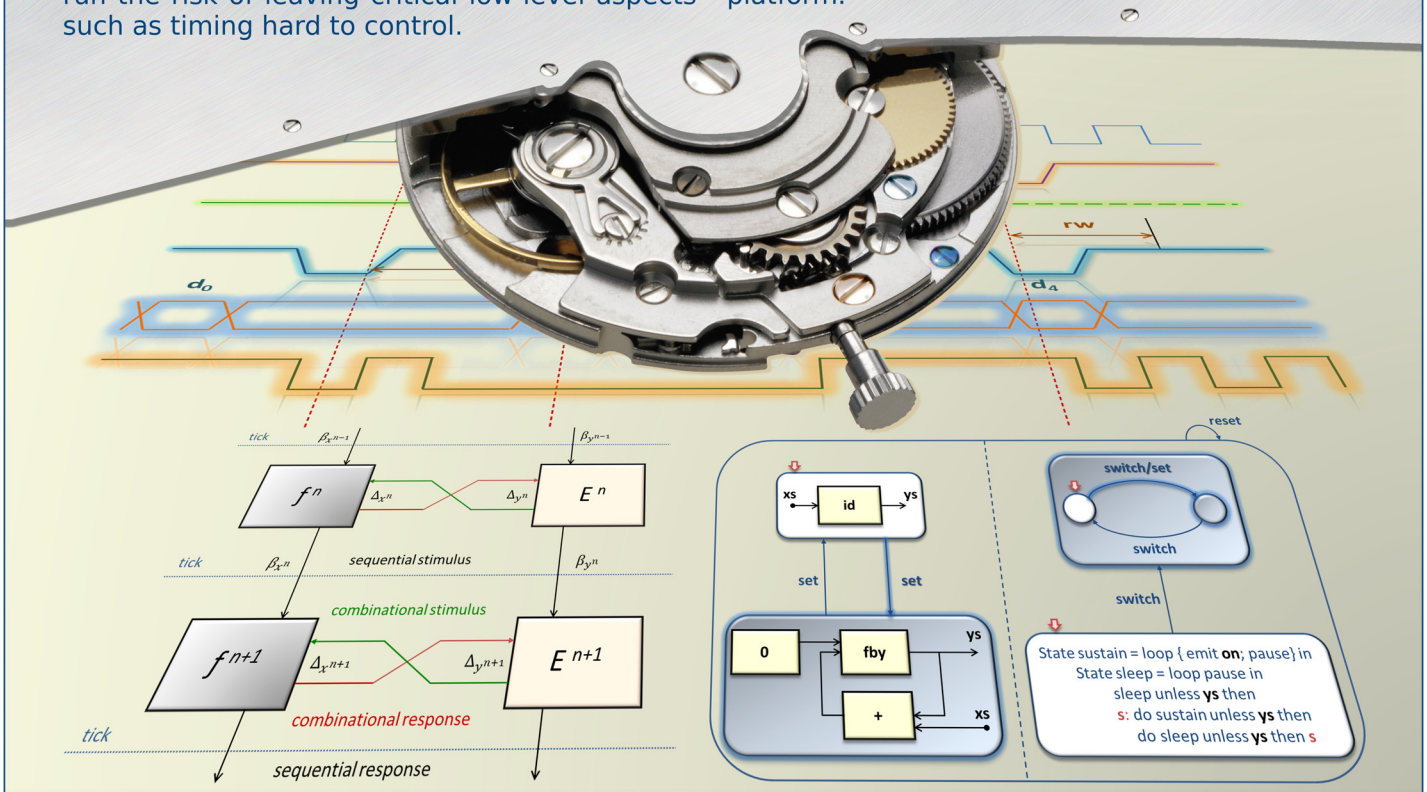
PRETSY: Precision Timed Reactive Processing

Embedded reactive real-time systems are ubiquitous today. They provide increasingly complex functionality, e.g. in modern avionics, automotive or medical products.

This rising complexity makes it important to apply high-level design approaches, yet they run the risk of leaving critical low-level aspects such as timing hard to control.

The PRETSY project investigates a novel, holistic approach for the design of timing-predictable and efficient reactive systems.

PRETSY encompasses both the modeling and programming levels, as well as the execution platform.



Predictable Control/Data Flow

- Synchronous Model of Computation
- Deterministic Clock-scheduled Execution

Predictable Instruction-level Timing

- Precision Timed Processing Architecture
- Worst-case Reaction Time

Holistic Model Based Design Flow and Tool Chain

- Synchronous Programming Language (SC Charts)
- Formal Semantical Basis
- Visual Design Capture (KIELER)
- Modular Compilation with Rich Interfaces
- Timing Analyzer and Clock Calculus
- Precision Timed (PRET) Architecture

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NATIONAL INSTRUMENTS

www.pretsy.org

DFG Deutsche Forschungsgemeinschaft