Port Constraints in Hierarchical Layout of Data Flow Diagrams

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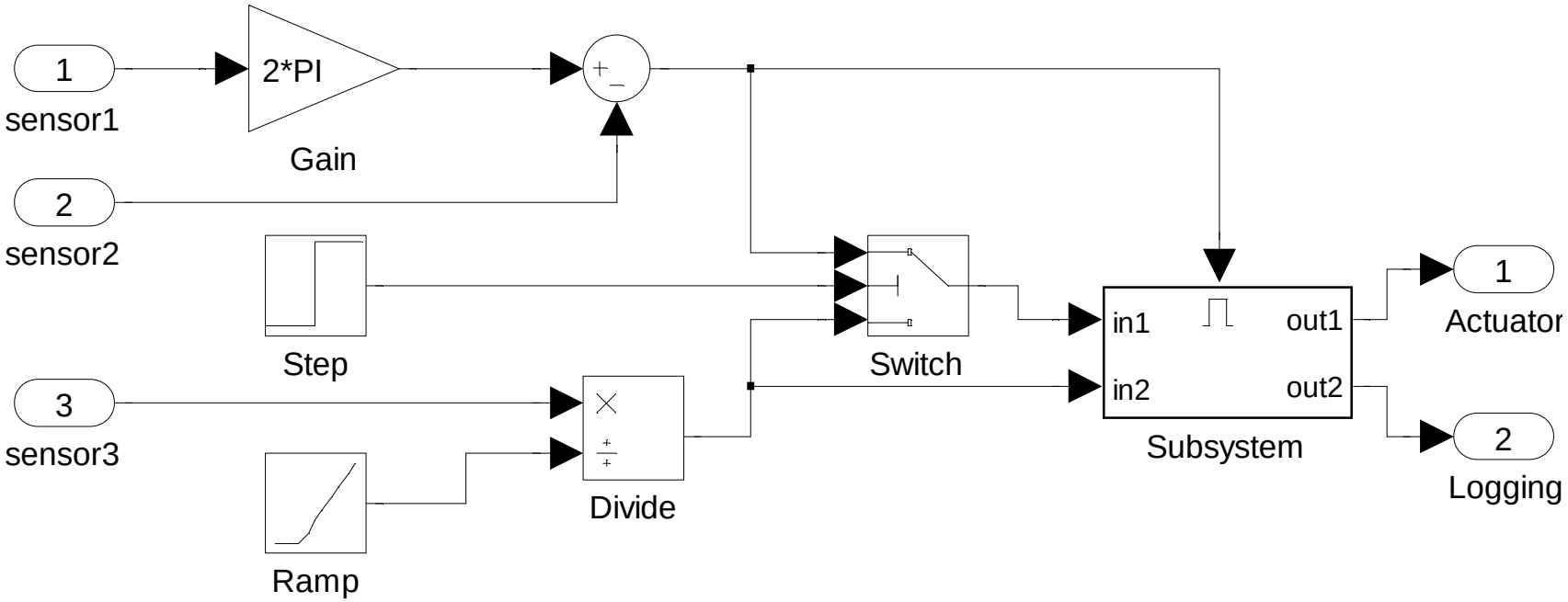
Graph Drawing 2009
September 24th

Outline

Data Flow Diagrams



- Graphical modeling languages for the design of complex (embedded) systems

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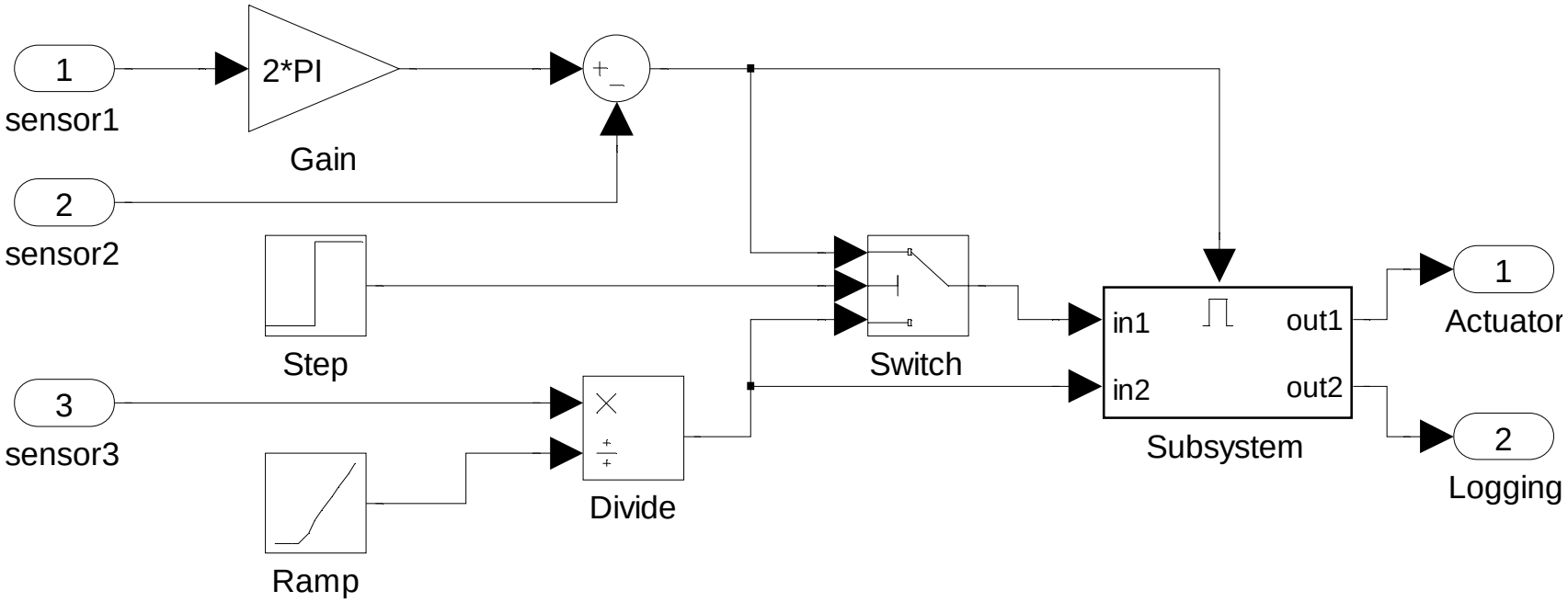

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- Employed in software and hardware development

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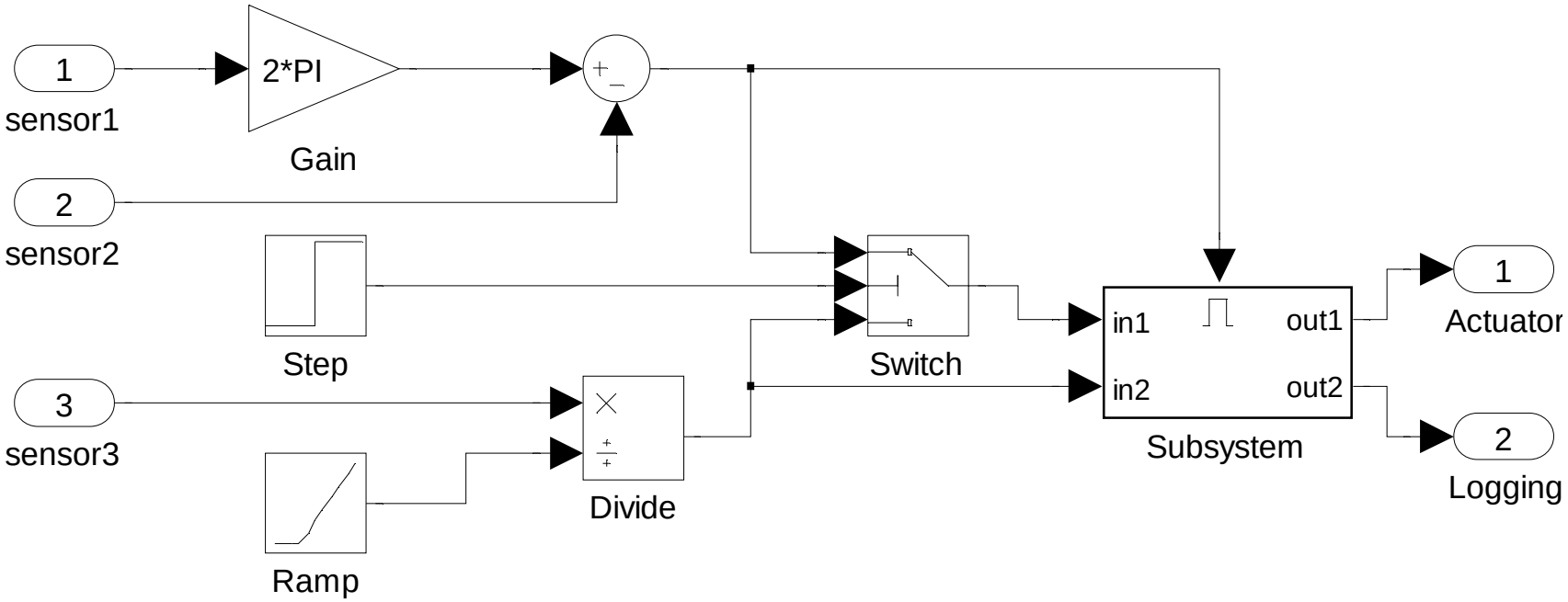
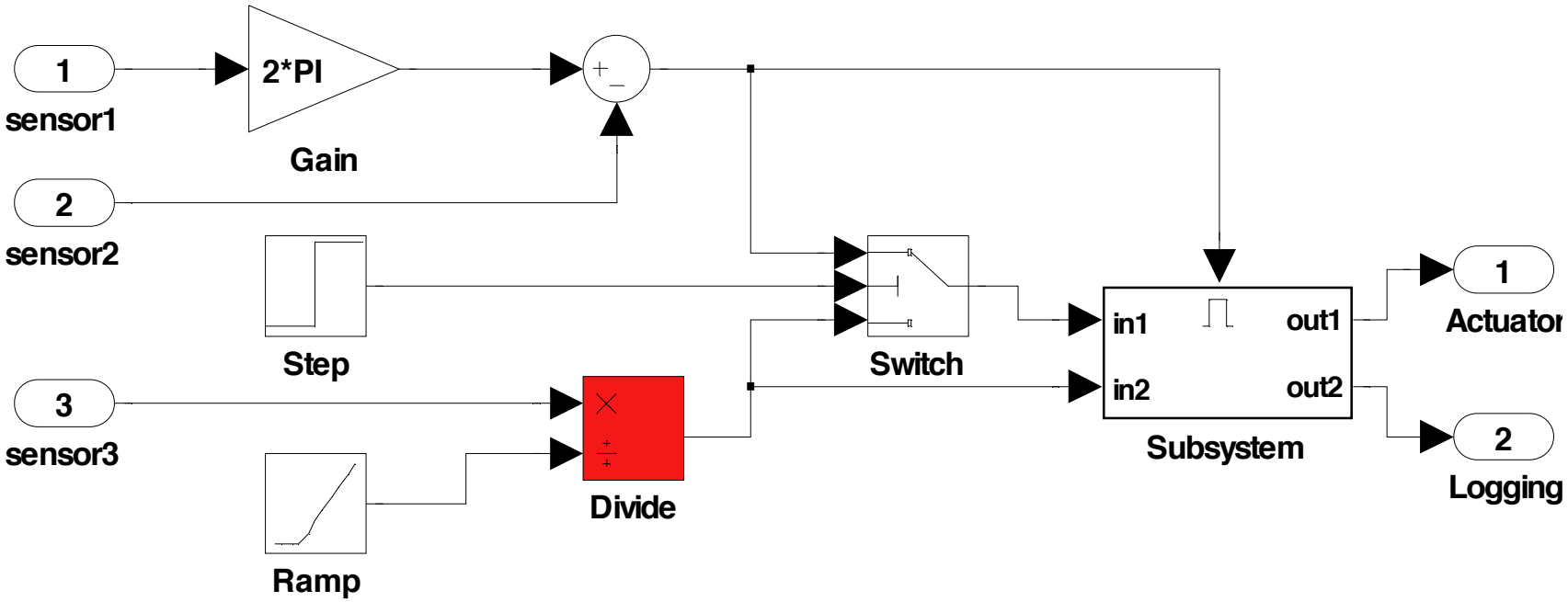


- Graphical modeling languages for the design of complex (embedded) systems
- Employed in software and hardware development
- Examples: Simulink, LabVIEW, ASCET, SCADE, Ptolemy

Data Flow Diagrams: Components



- Vertices: operators that produce and consume data

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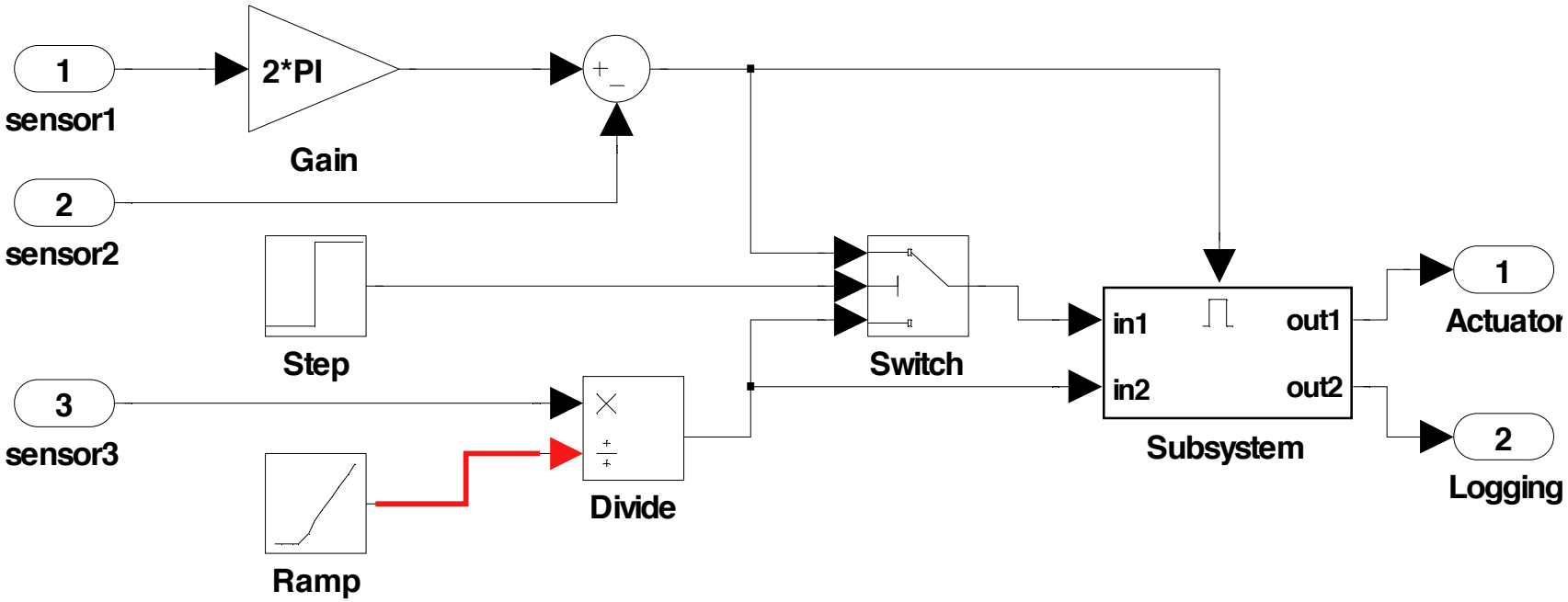

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- Edges: data paths between operators (orthogonal, left to right)

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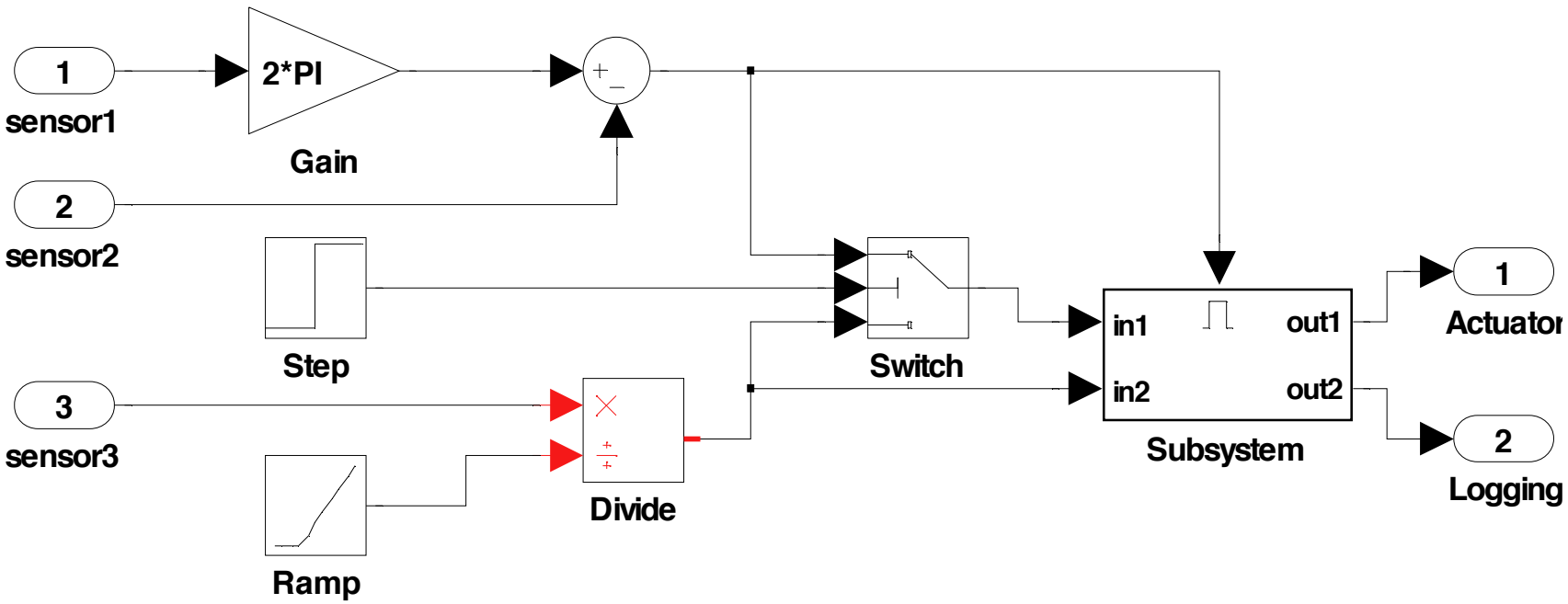

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- Ports: interface of the operators
  - Input ports mostly on left side, output ports on right side

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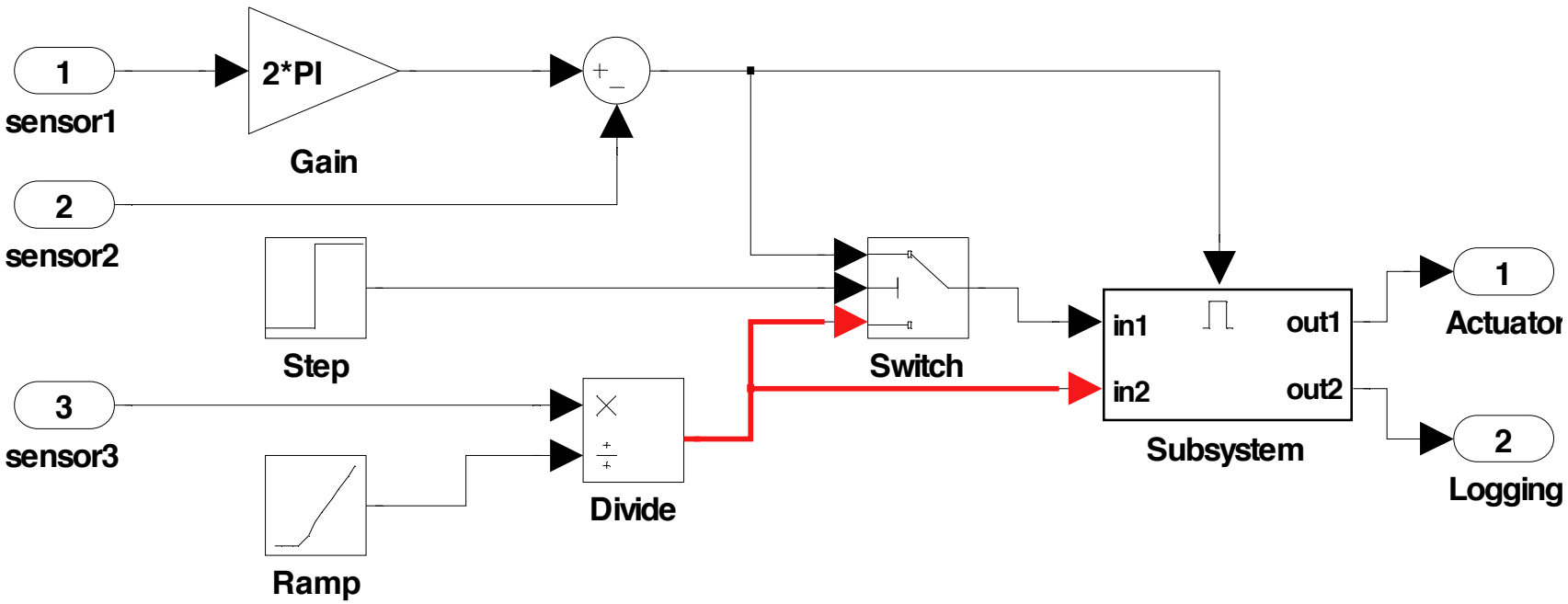
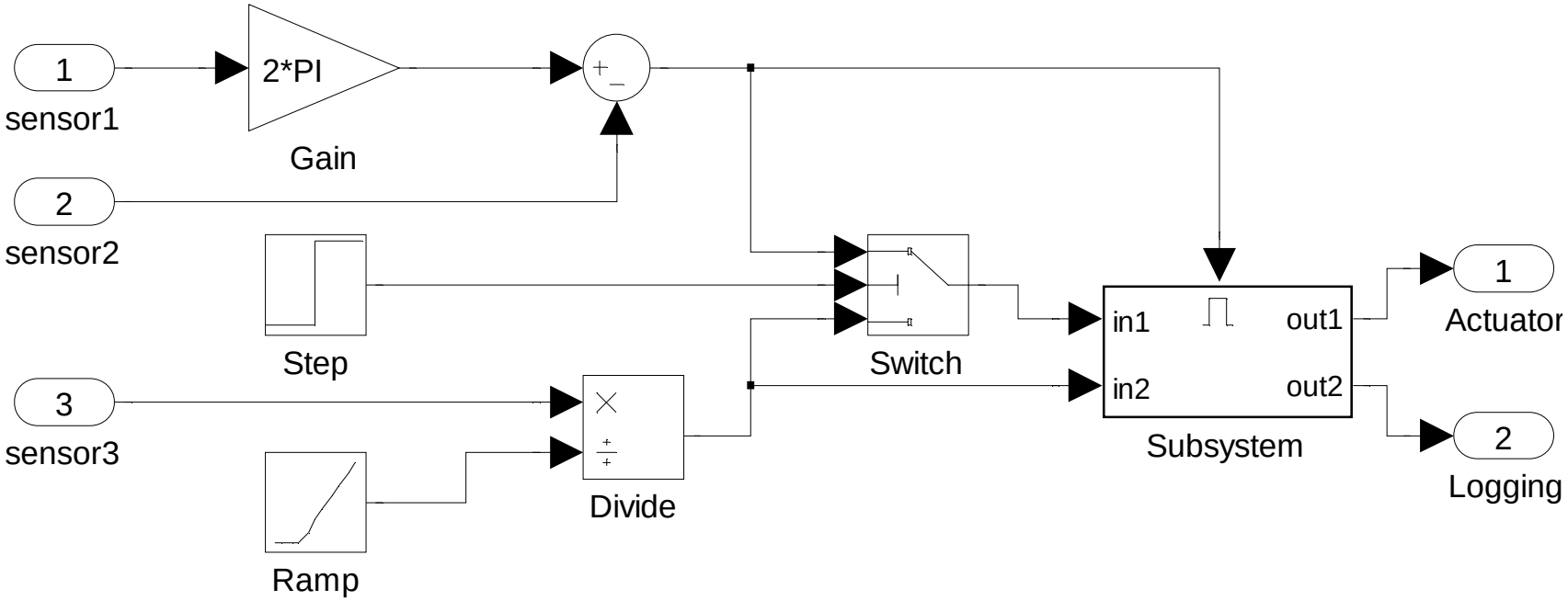


- Vertices: operators that produce and consume data
- Edges: data paths between operators (orthogonal, left to right)
- Ports: interface of the operators
  - Input ports mostly on left side, output ports on right side
- Multiple target ports lead to hyperedges

Data Flow Diagrams: Automatic Layout



- Most data flow modeling tools do not offer automatic layout

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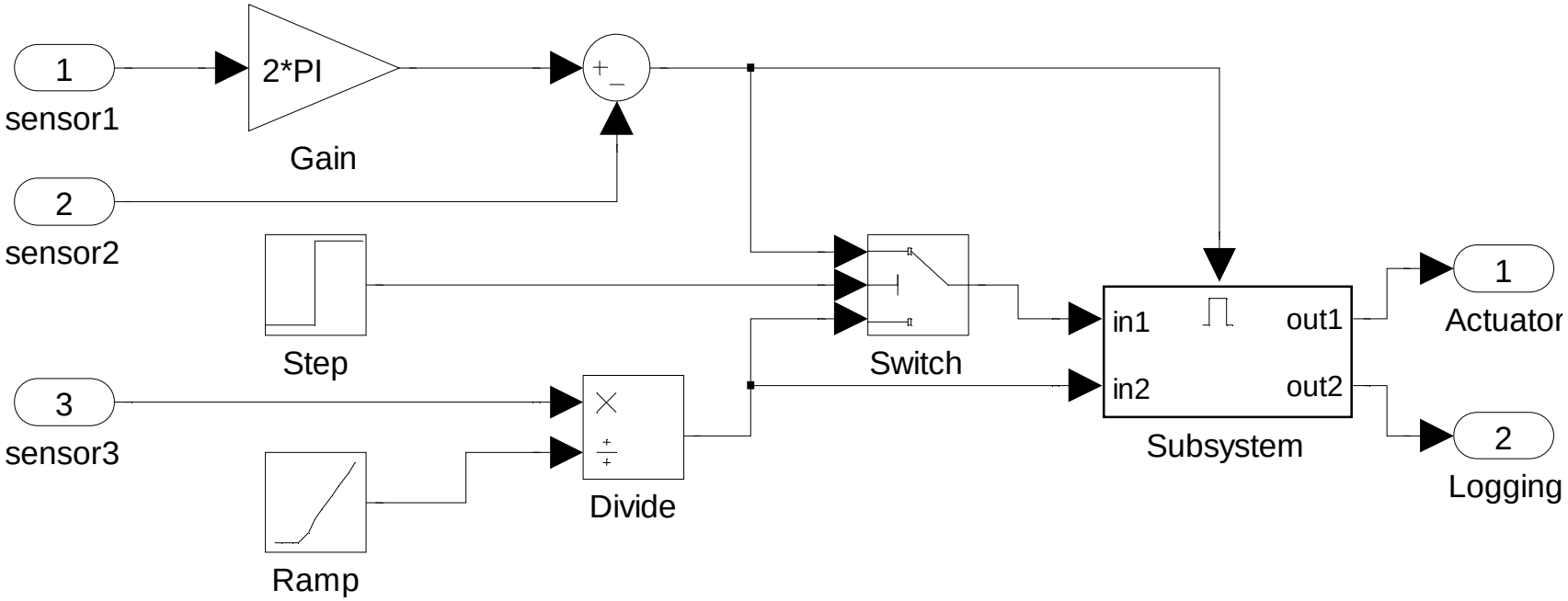

- Most data flow modeling tools do not offer automatic layout
- Standard layout algorithms cannot be applied
  - Need to extend for handling of ports and hyperedges

Port Constraints

Four scenarios for constraints on port positions:

Port Constraints

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1. Free ports: arbitrary positions on the node's border

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Four scenarios for constraints on port positions:

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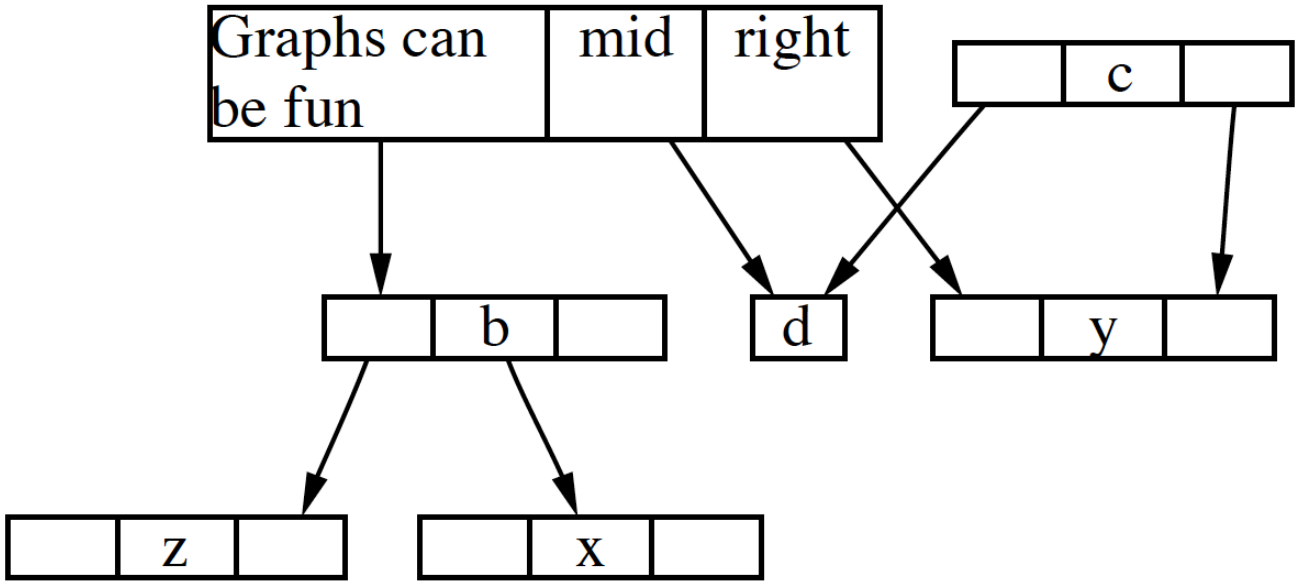
4. Fixed ports: fixed exact positions on the node's border

Port Constraints: Previous Work



E. R. Gansner, E. Koutsofios, S. C. North, K. Vo. *A technique for drawing directed graphs*, 1993.

- Gansner et al. 1993: port displacements for vertex placement

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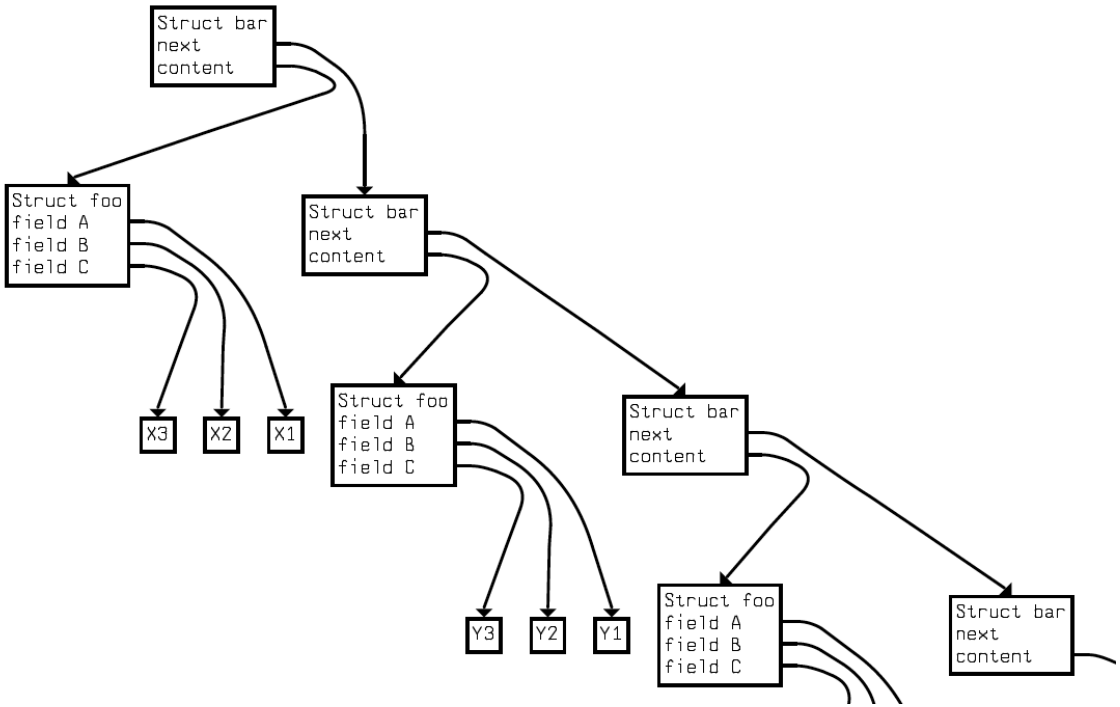

G. Sander. *Graph layout through the VCG tool*, 1994.

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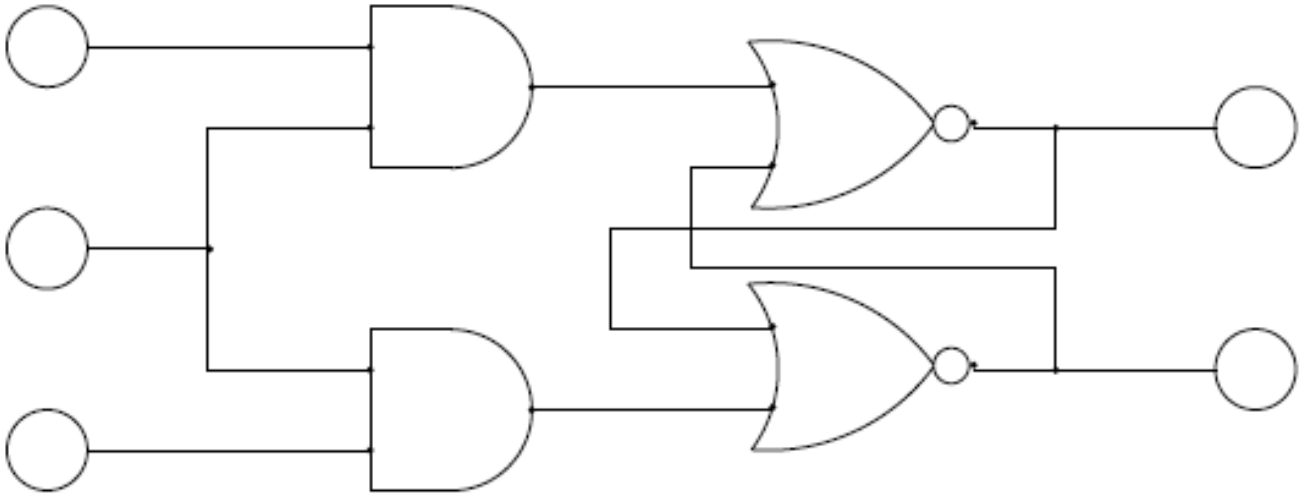

T. Eschbach. *Visualisierungen im Schaltkreisentwurf*, 2008.

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- Layout of circuit schematics: similar problem

Port Constraints: Previous Work

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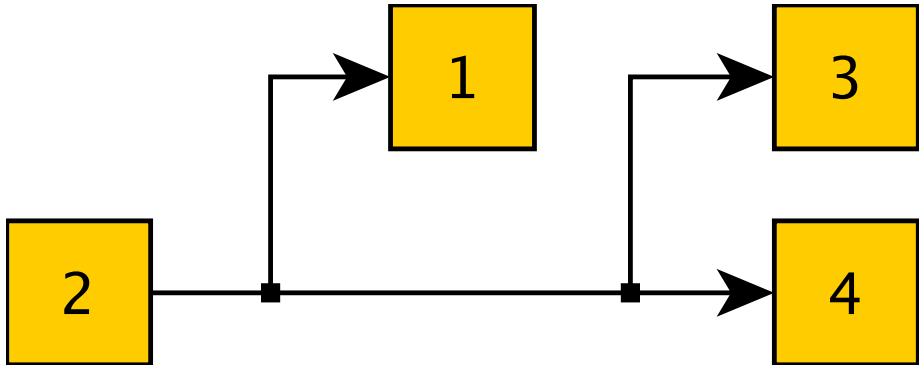
- Sander 1994: anchor points of edges
- Layout of circuit schematics: similar problem
- Some commercial layout libraries support port constraints, no details published

Hyperedges



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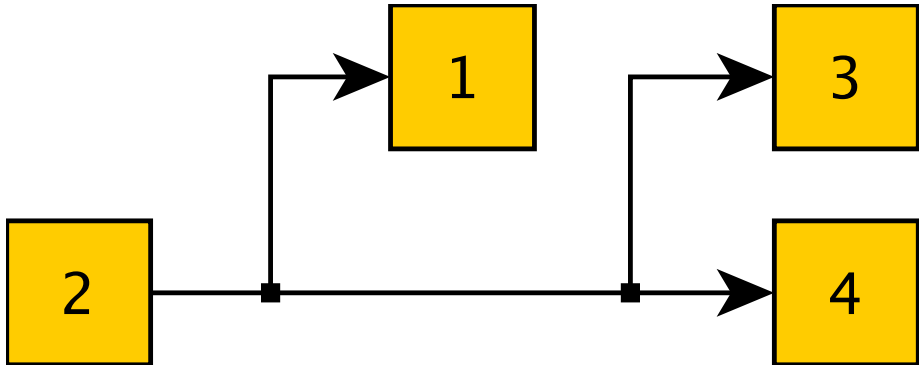
Hyperedges



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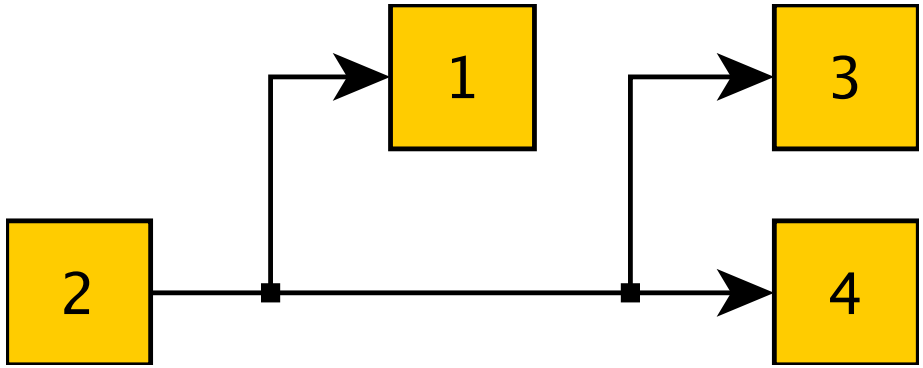

- One approach: handle hyperedges directly
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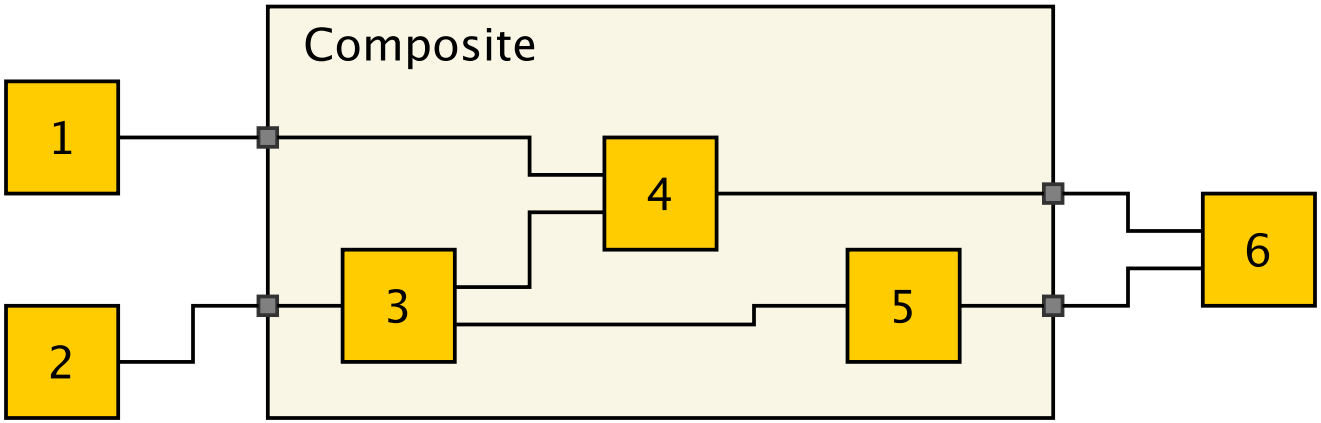
- Simpler approach: replace by a set of normal edges, e.g. $(2, 1)$, $(2, 3)$, $(2, 4)$
- Not unique for multiple sources *and* multiple targets, but OK for most data flow diagrams

Compound Diagrams



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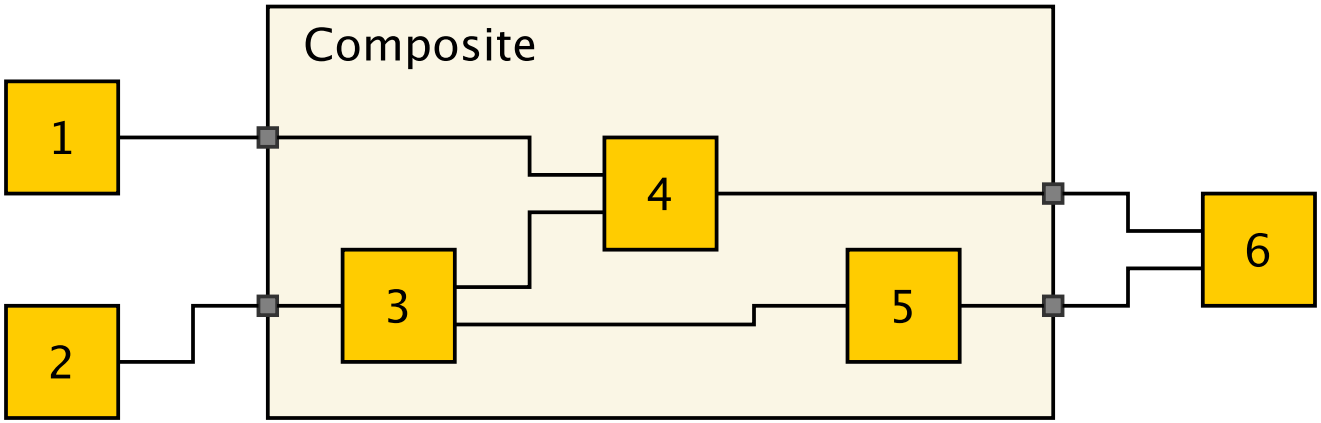
Compound Diagrams



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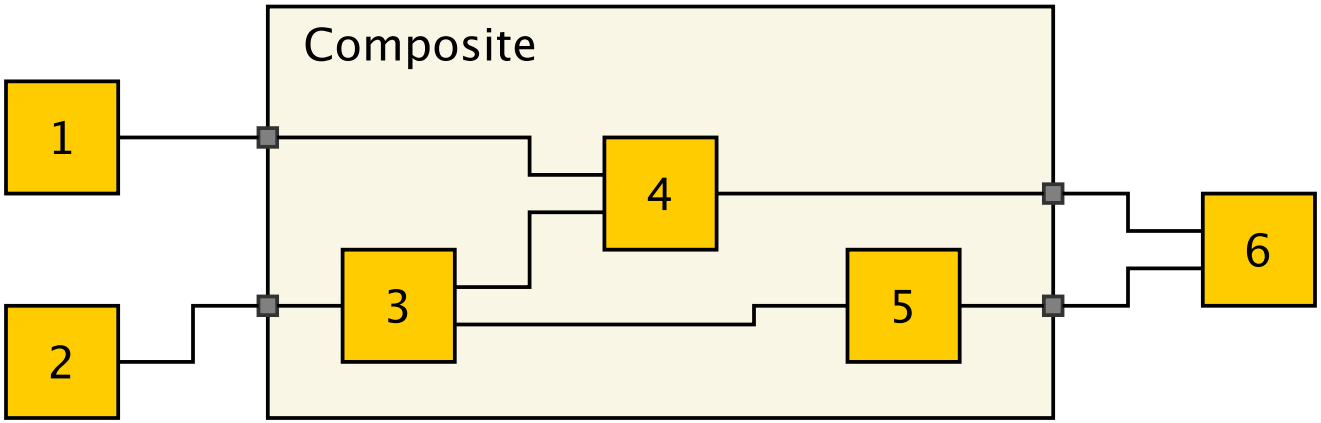

- Compound operators may contain nested diagrams
- There are approaches to handle general compound graphs
  - Sugiyama et al. 1991, Sander 1996
- Different situation: edges do not cross vertex boundaries, but may be connected with external ports

1. Introduction – Problem Statement and Related Work
   - Data Flow Diagrams
   - Port Constraints
   - Hyperedges
   - Compound Diagrams

2. Extensions of Hierarchical Layout
   - Assignment of Dummy Vertices
   - Crossing Minimization
   - Orthogonal Edge Routing

3. Results
   - Layout Gallery
   - Applications and Demonstration

The Hierarchical Approach

Steps of our variant of the hierarchical layout algorithm:

1. Cycle removal
2. Layer assignment
3. Crossing minimization
4. Edge routing I
5. Vertex placement
6. Edge routing II

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- Main contributions are in the highlighted steps

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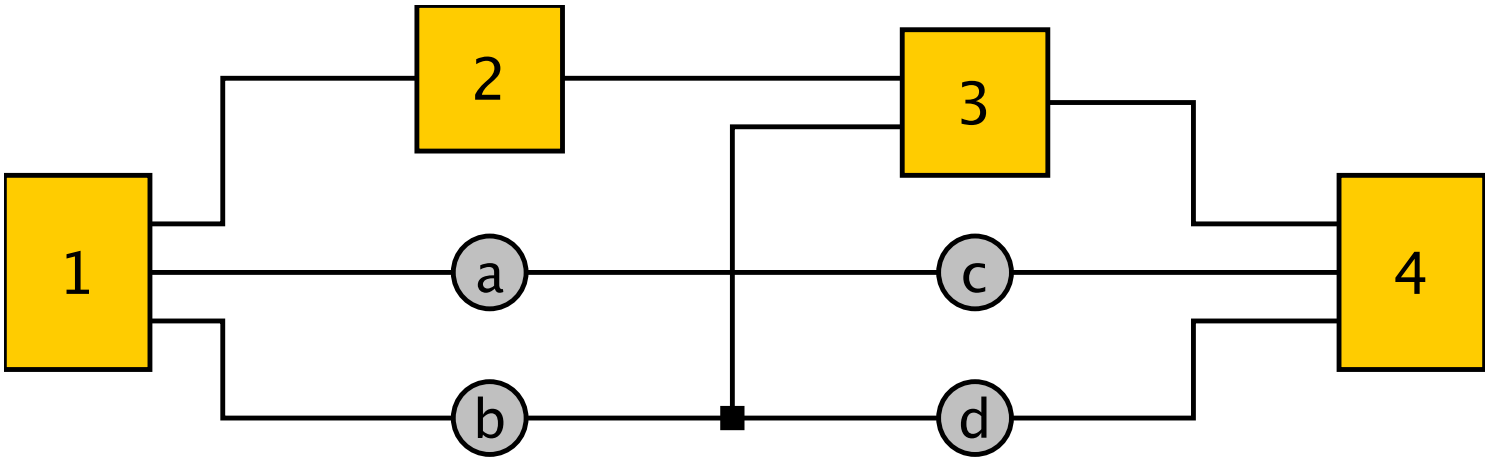
Steps of our variant of the hierarchical layout algorithm:

1. Cycle removal
2. **Layer assignment**
3. **Crossing minimization**
4. **Edge routing I**
5. Vertex placement
6. Edge routing II

- Main contributions are in the highlighted steps
- Standard methods for other steps
  - G. Di Battista, P. Eades, R. Tamassia, I. G. Tollis 1999
  - Sander 1996, 2004

Step 2: Assignment of Dummy Vertices



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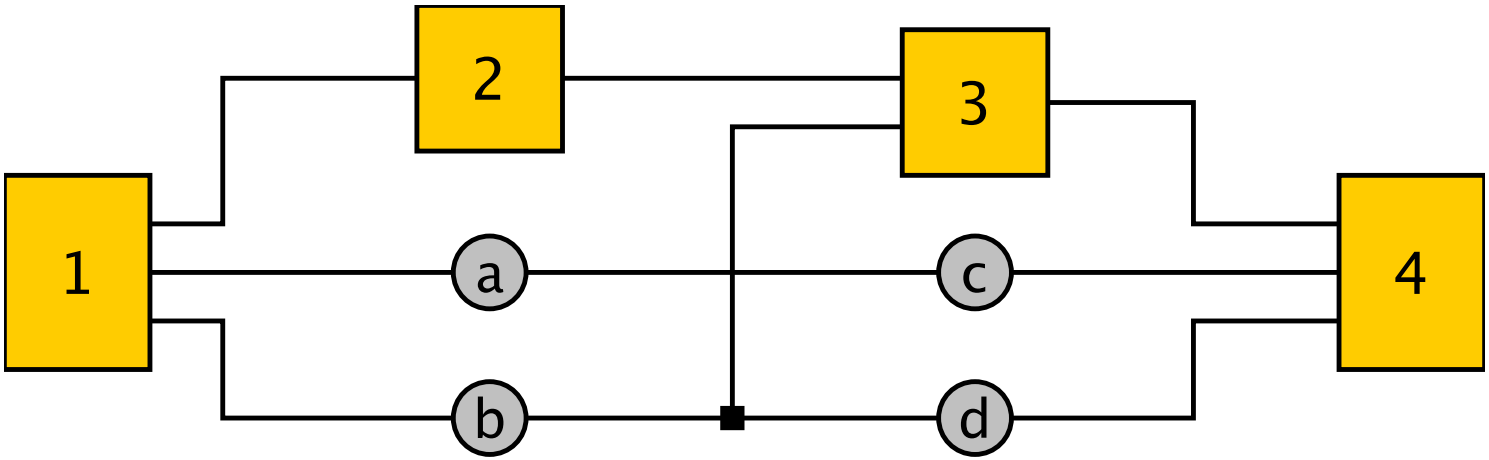

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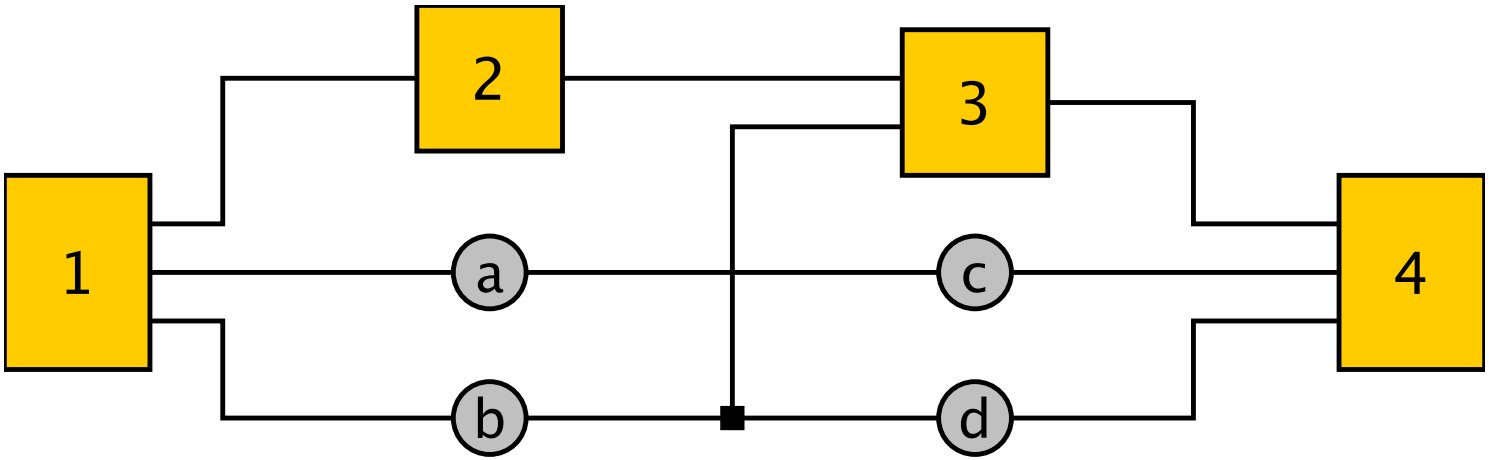
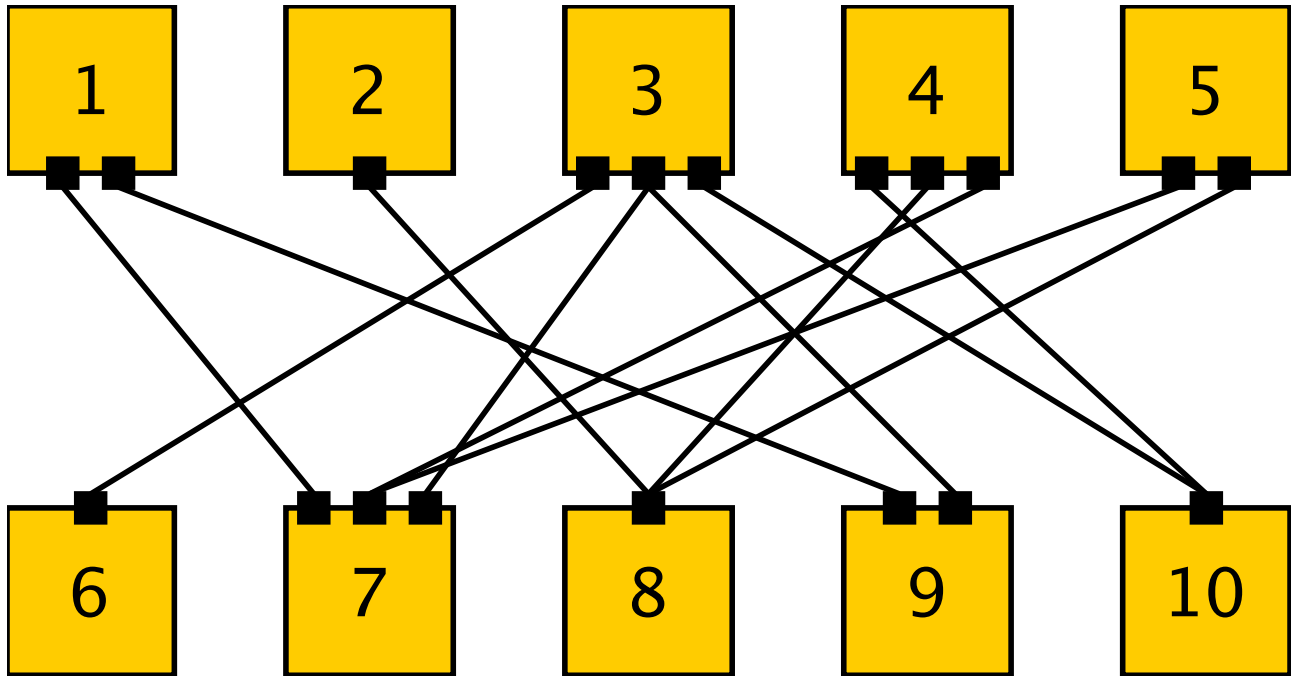


- A standard method is used for assigning vertices to layers
- Dummy vertices are used to split long edges
- Merge dummy vertices of long edges that belong to the same hyperedge
  - Edges $(1, 3)$ and $(1, 4)$ share the dummy vertex b

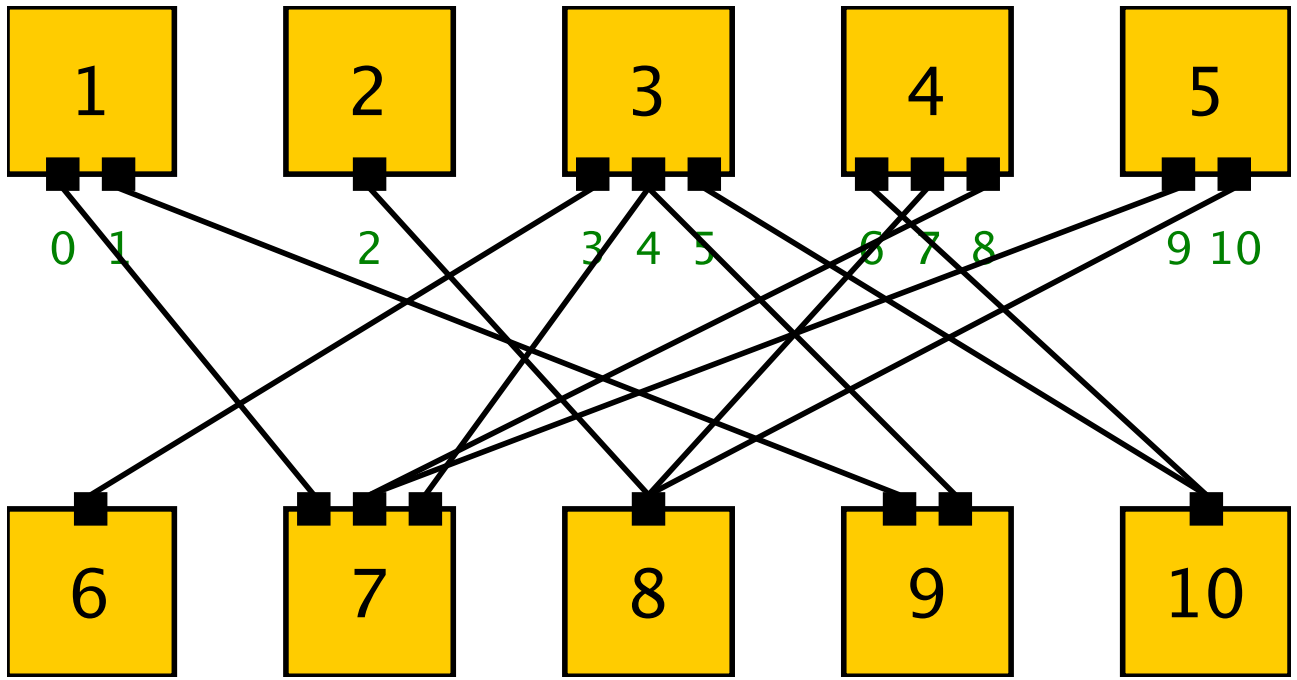
Step 3: Crossing Minimization

- Use two-layer crossing minimization method for layer-by-layer sweep



Step 3: Crossing Minimization: Barycenter Method

- Extended barycenter method: determine port ranks in the fixed layer



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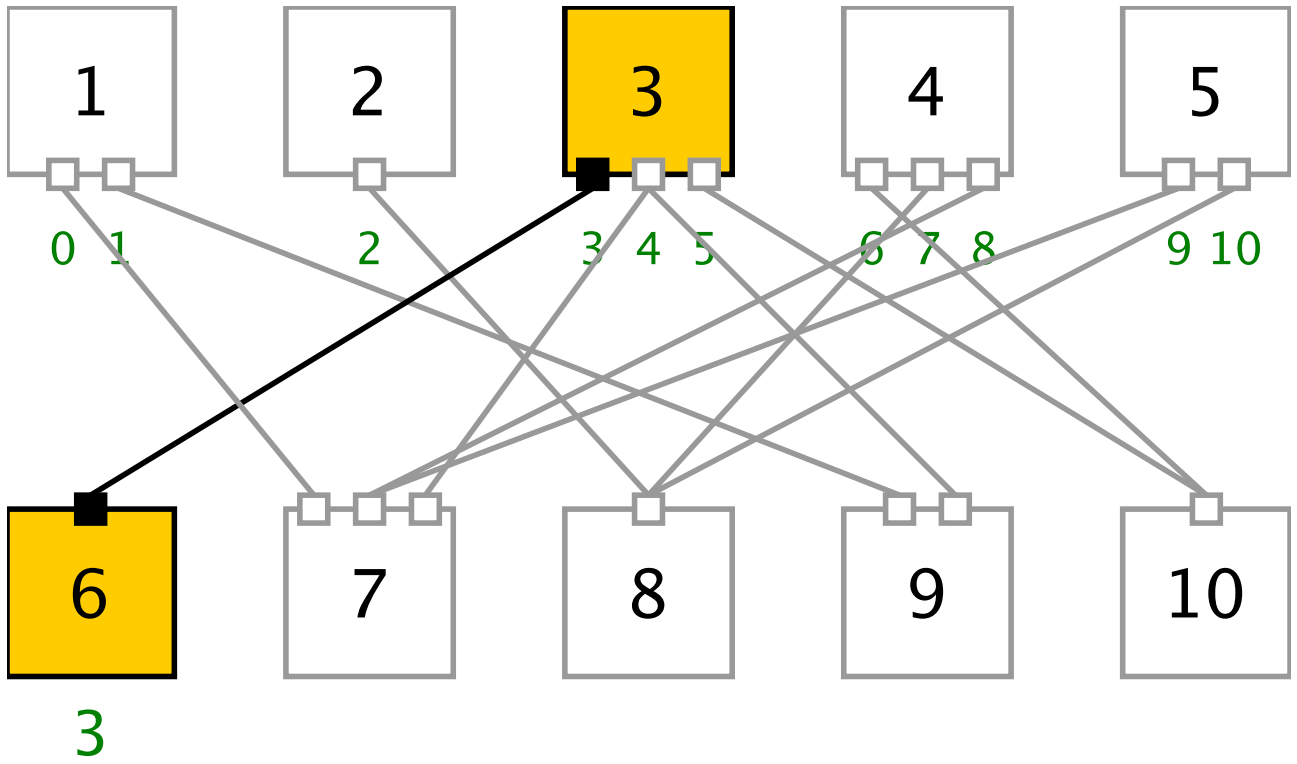
- Calculate barycenter values as average of the ranks of connected ports for all nodes in the free layer



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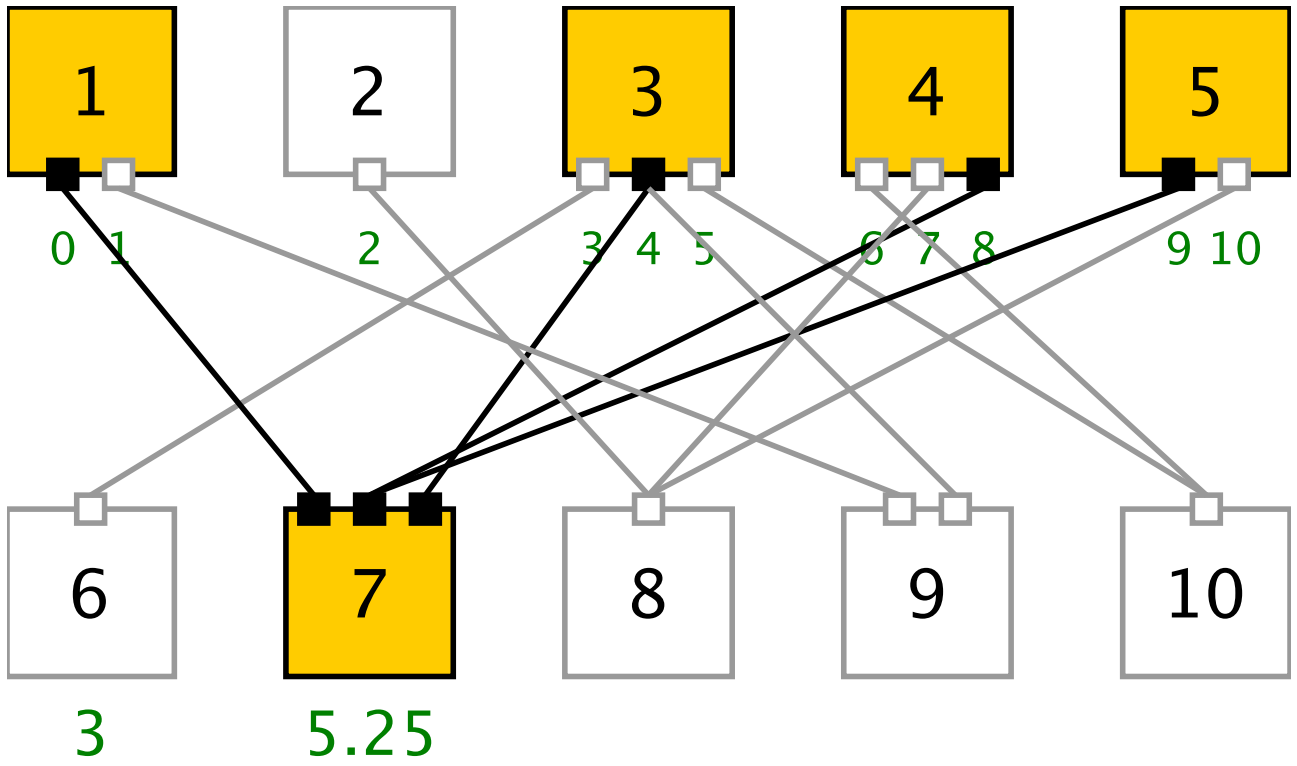

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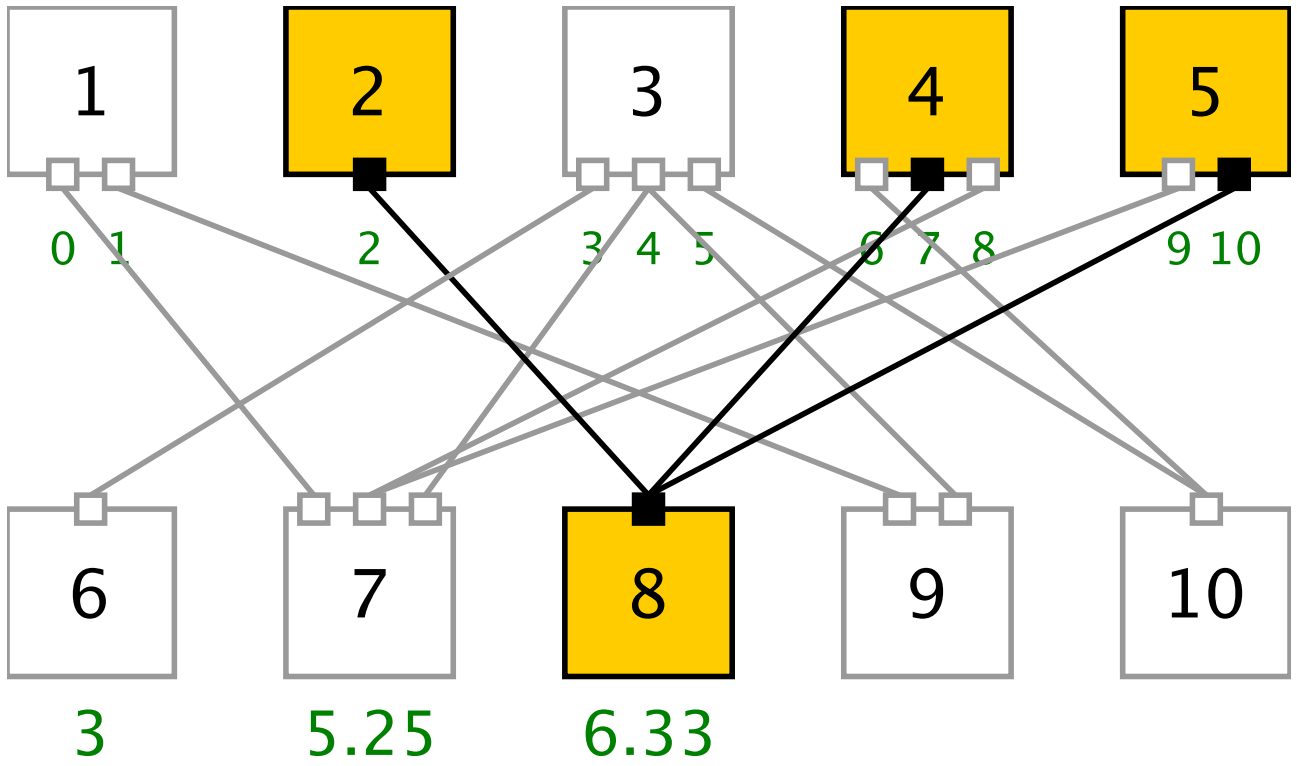

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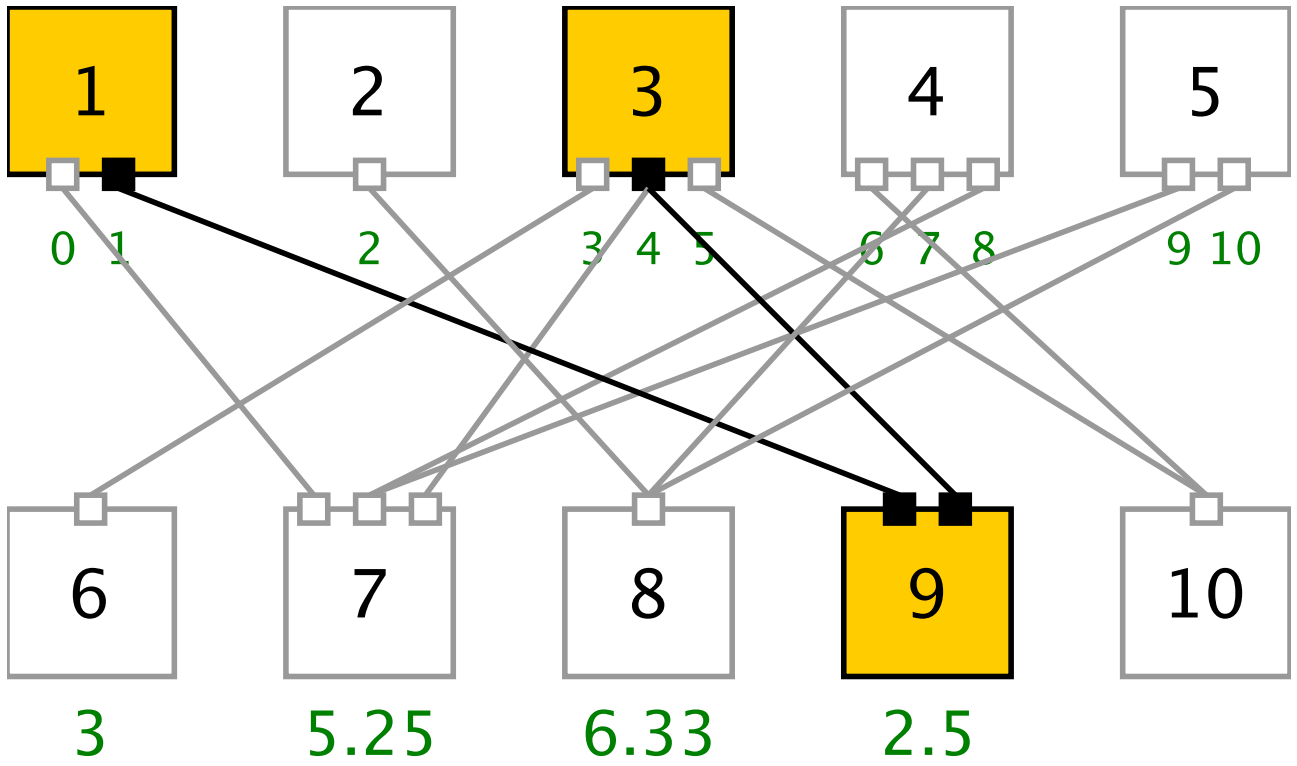

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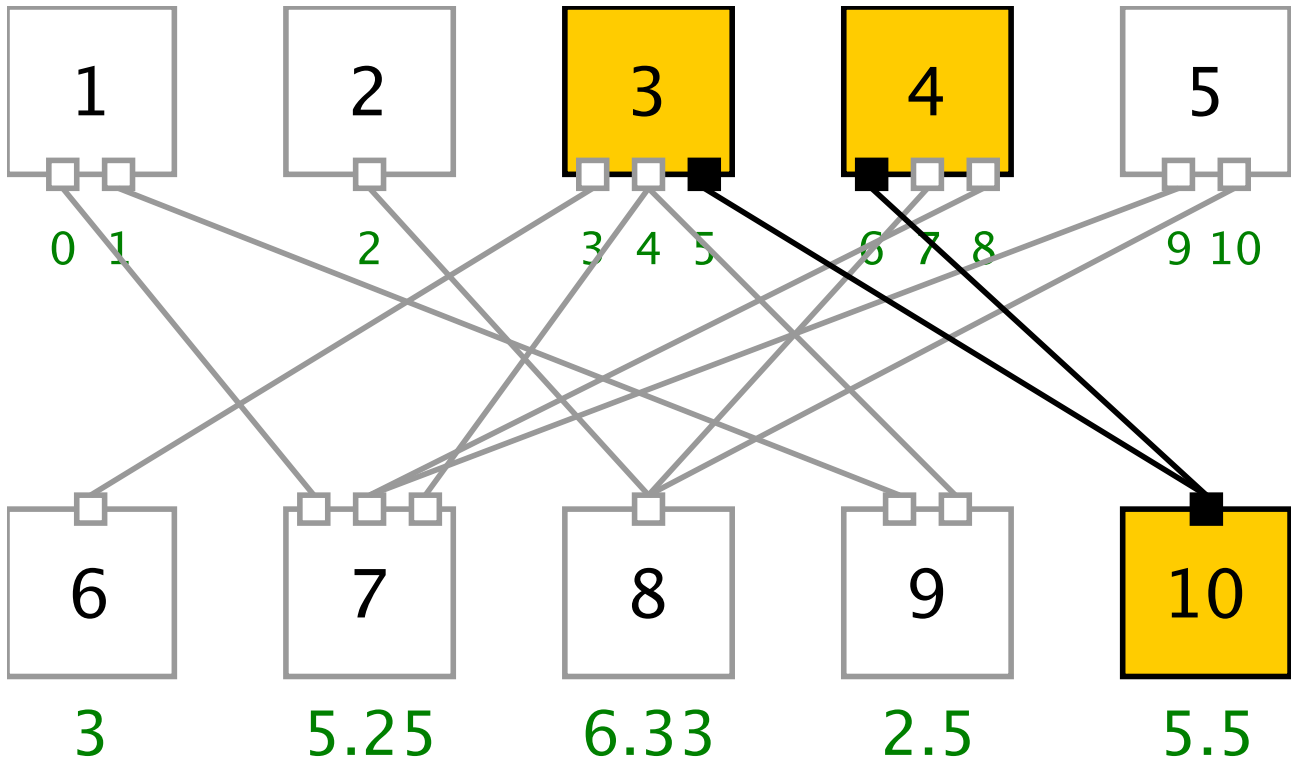
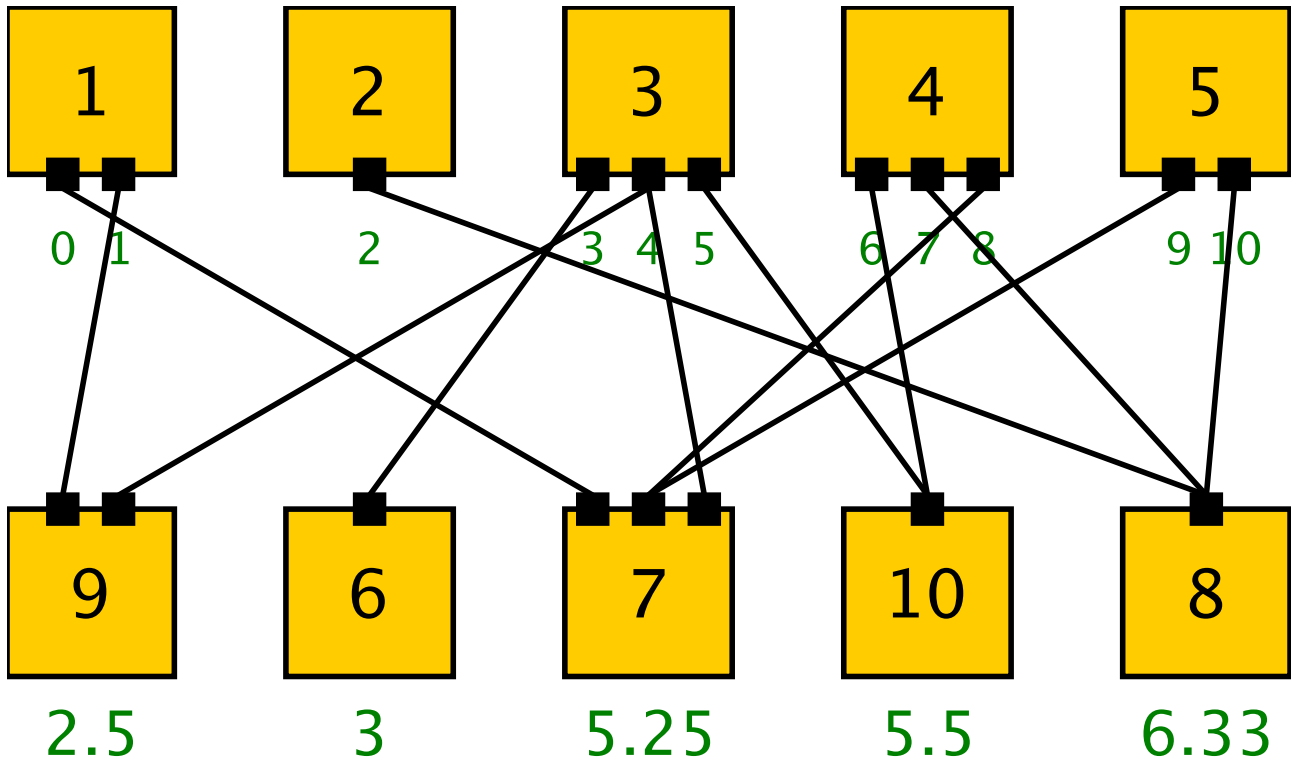
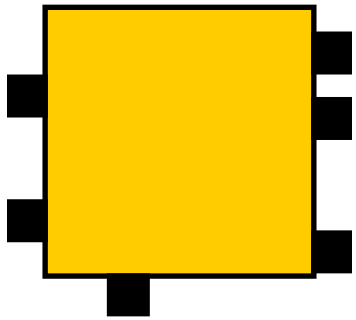


Step 3: Crossing Minimization: Barycenter Method

- Order the nodes in the free layer by their barycenter values



Scenarios of Port Constraints



- Fixed ports: use extended barycenter method

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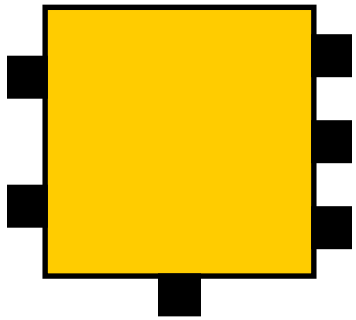

- Fixed ports: use extended barycenter method
- Fixed port order: as with fixed ports; distribute ports evenly on the vertex border first

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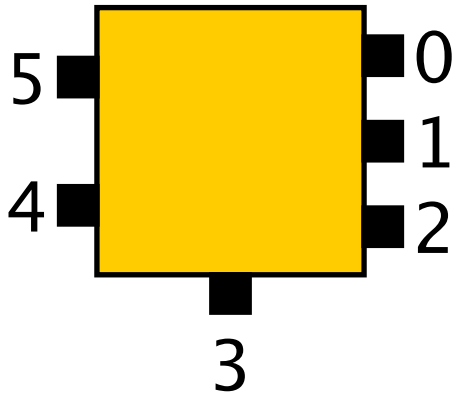

- Fixed ports: use extended barycenter method
- Fixed port order: as with fixed ports; distribute ports evenly on the vertex border first
- Fixed sides: set order of ports for each vertex using the extended barycenter method
  - Determine vertex barycenters from their port barycenters

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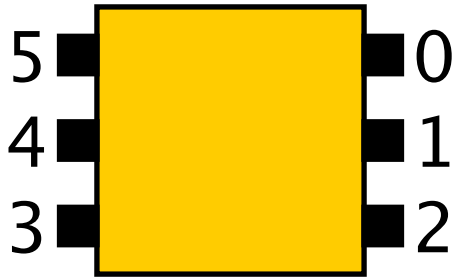

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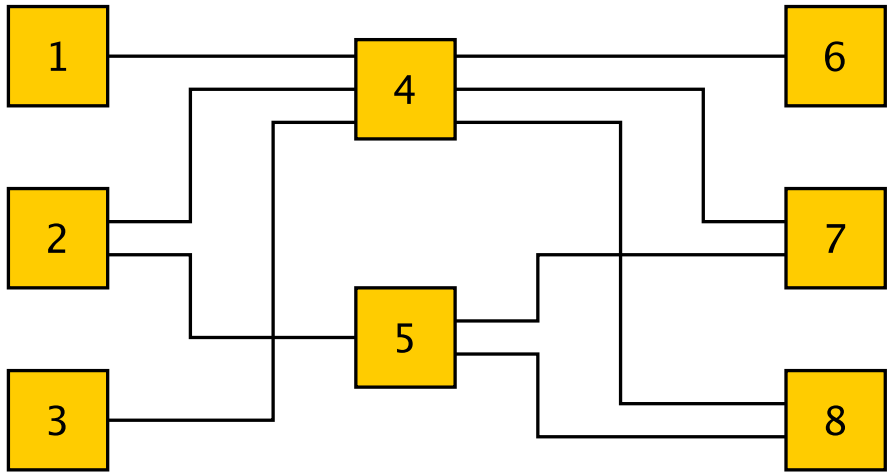
- Fixed port order: as with fixed ports; distribute ports evenly on the vertex border first
- Fixed sides: set order of ports for each vertex using the extended barycenter method
  - Determine vertex barycenters from their port barycenters
- Free ports: as with fixed sides; first put input ports left, output ports right

Orthogonal Edge Routing



- Create appropriate horizontal and vertical line segments

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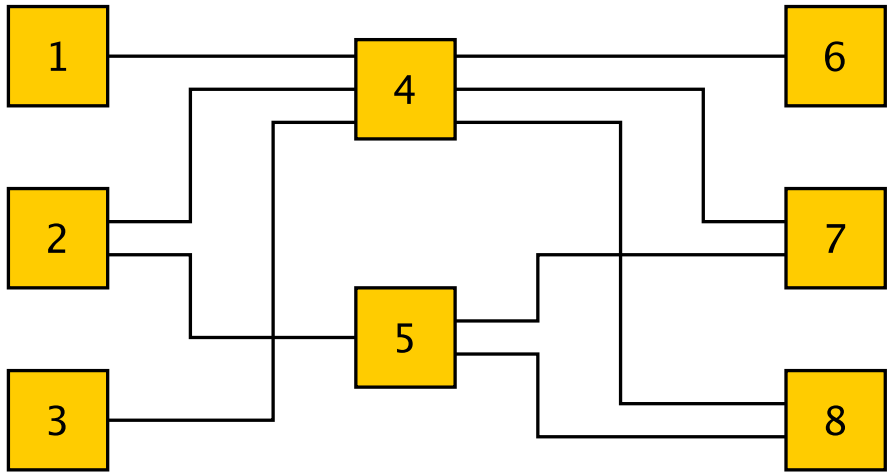

- Create appropriate horizontal and vertical line segments
- Can apply standard methods if the source port is on the right side and target port is on the left side
  - Eschbach et al. 2006, Sander 1996, Baburin 2002

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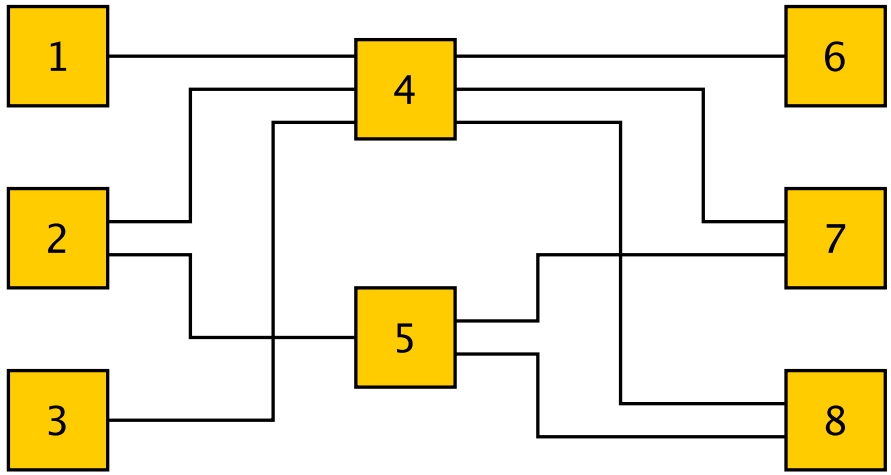
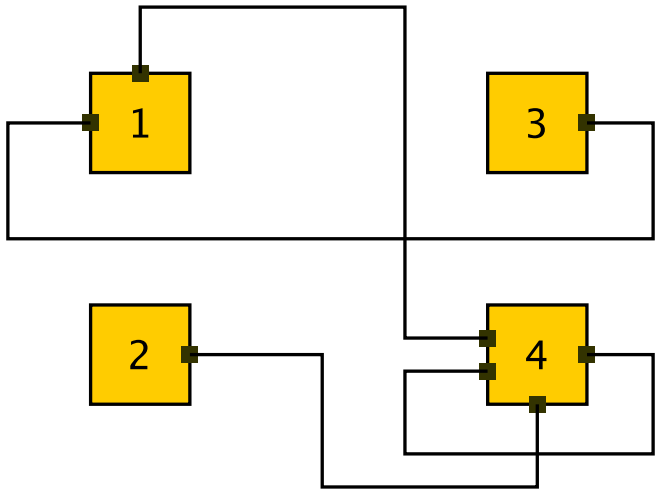


- Create appropriate horizontal and vertical line segments
- Can apply standard methods if the source port is on the right side and target port is on the left side
  - Eschbach et al. 2006, Sander 1996, Baburin 2002
- What about ports on other sides?

Step 4: Routing Around Vertices



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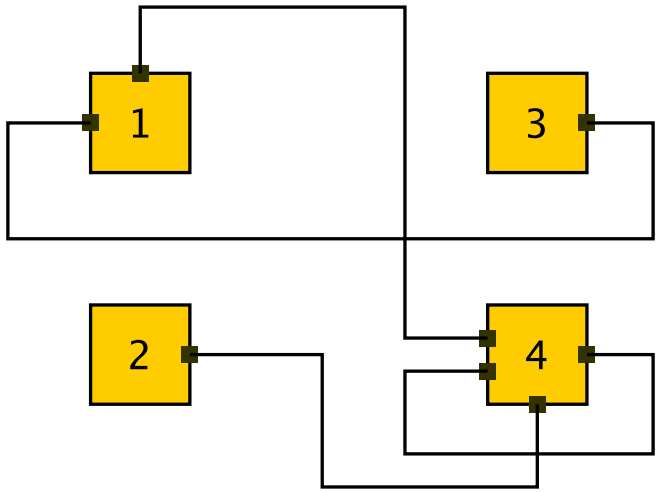
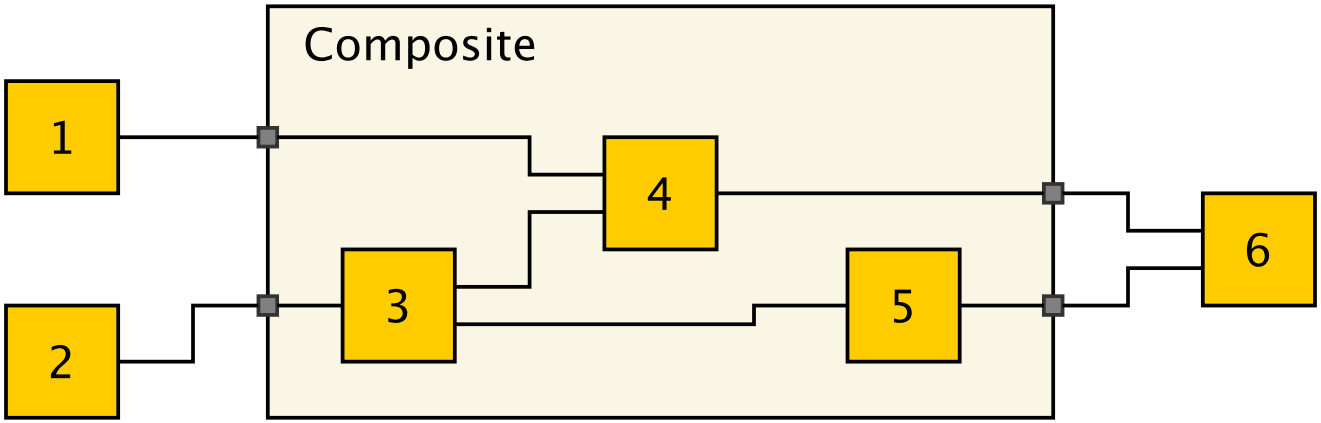


- Need to route edges around vertices
- Apply additional routing step after crossing minimization
  - Order the edges appropriately
  - Determine amount of space needed for the edges, use this information in the subsequent vertex placement step

Step 6: Routing to External Ports



- If a compound diagram has connections to external ports, they must be properly routed

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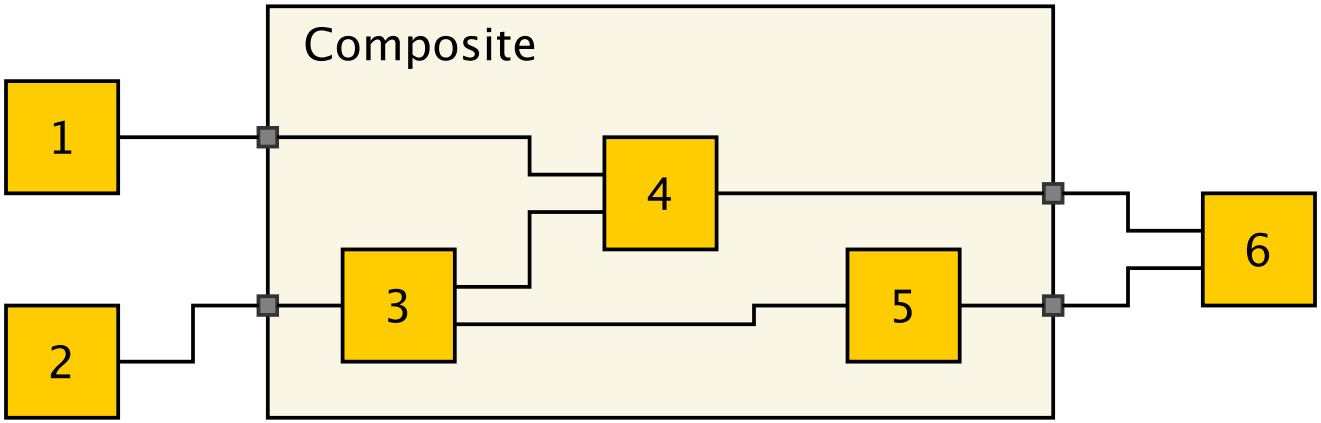

- If a compound diagram has connections to external ports, they must be properly routed
- General approach: apply layout recursively
  - Treat external ports as ordinary vertices in most steps of the algorithm
  - Input ports to the first layer, output ports to the last layer
  - Need special handling to place ports on the border of the parent vertex and route connected edges

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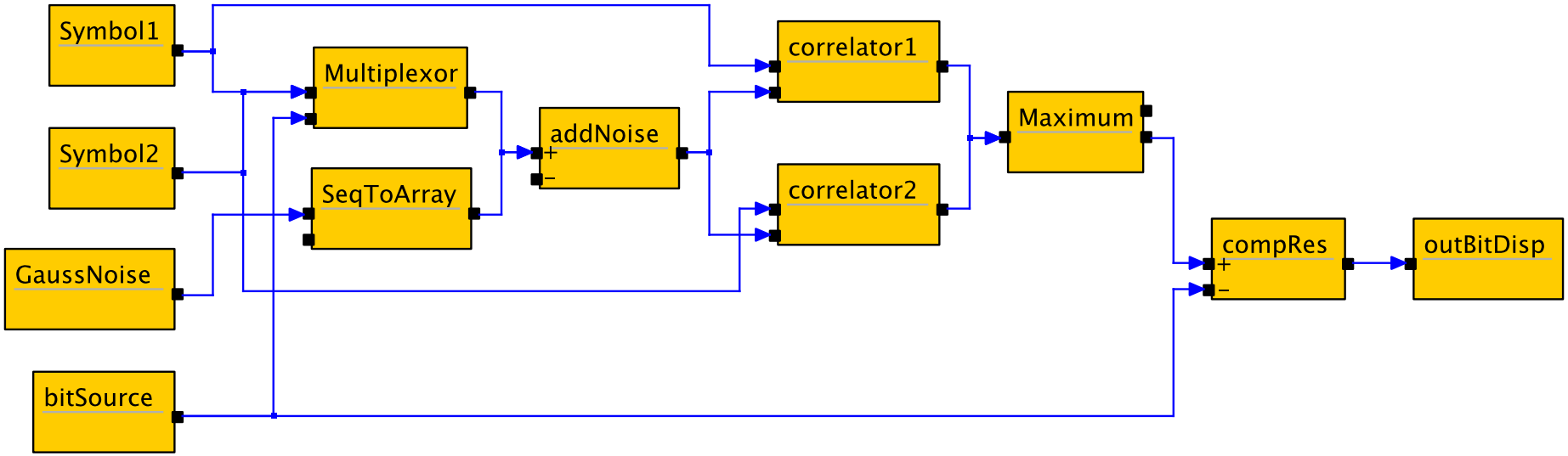
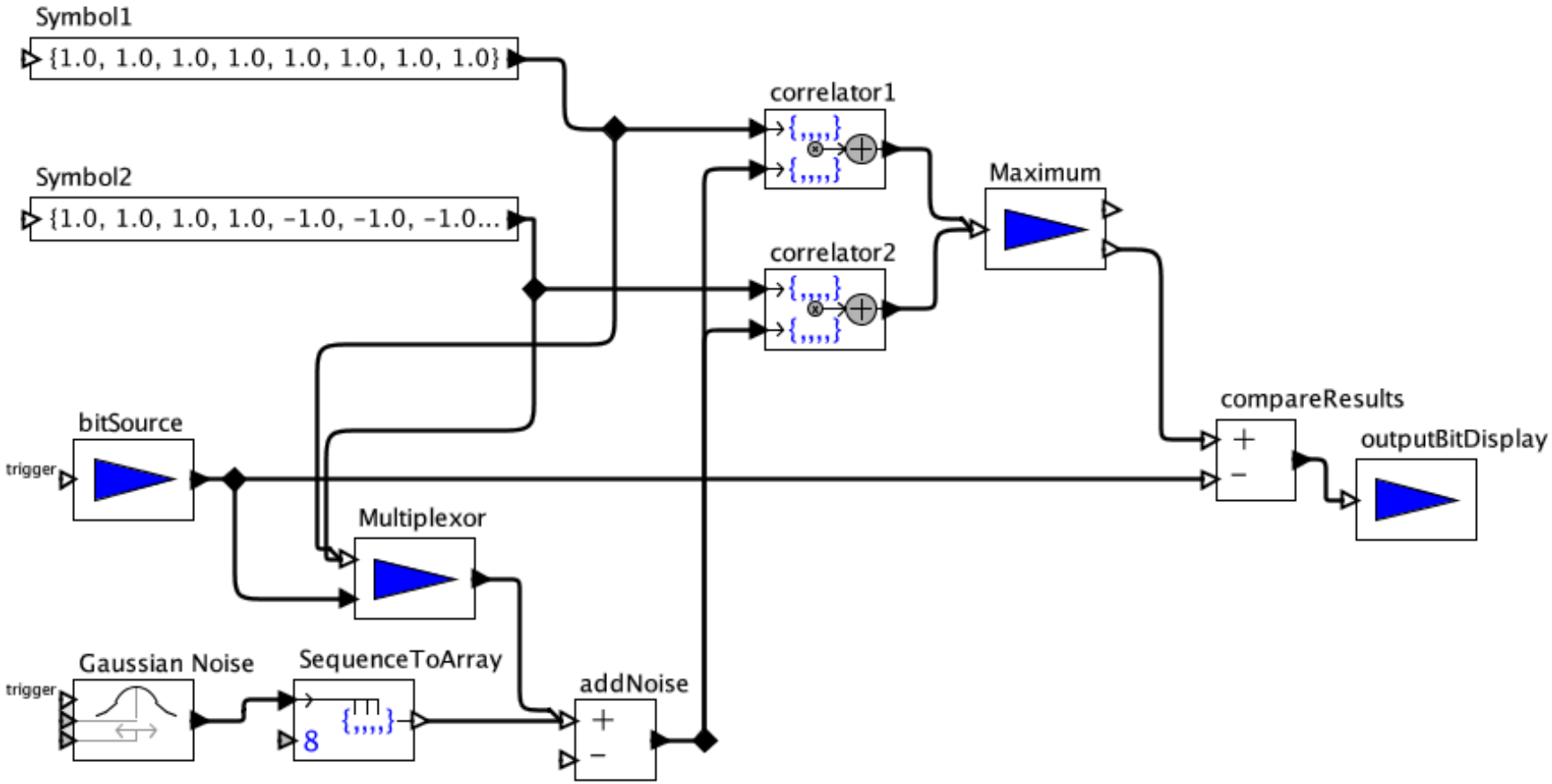
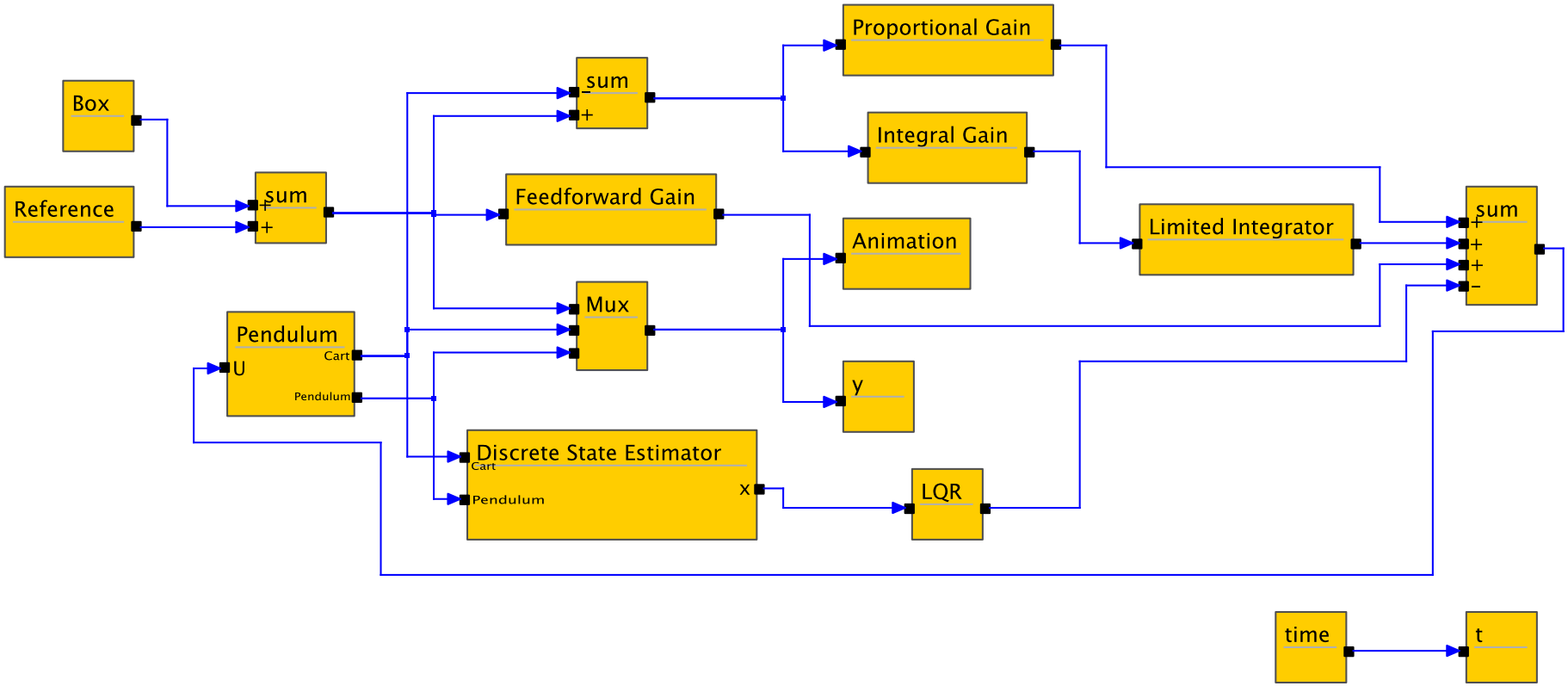
Layout Gallery (1/5)



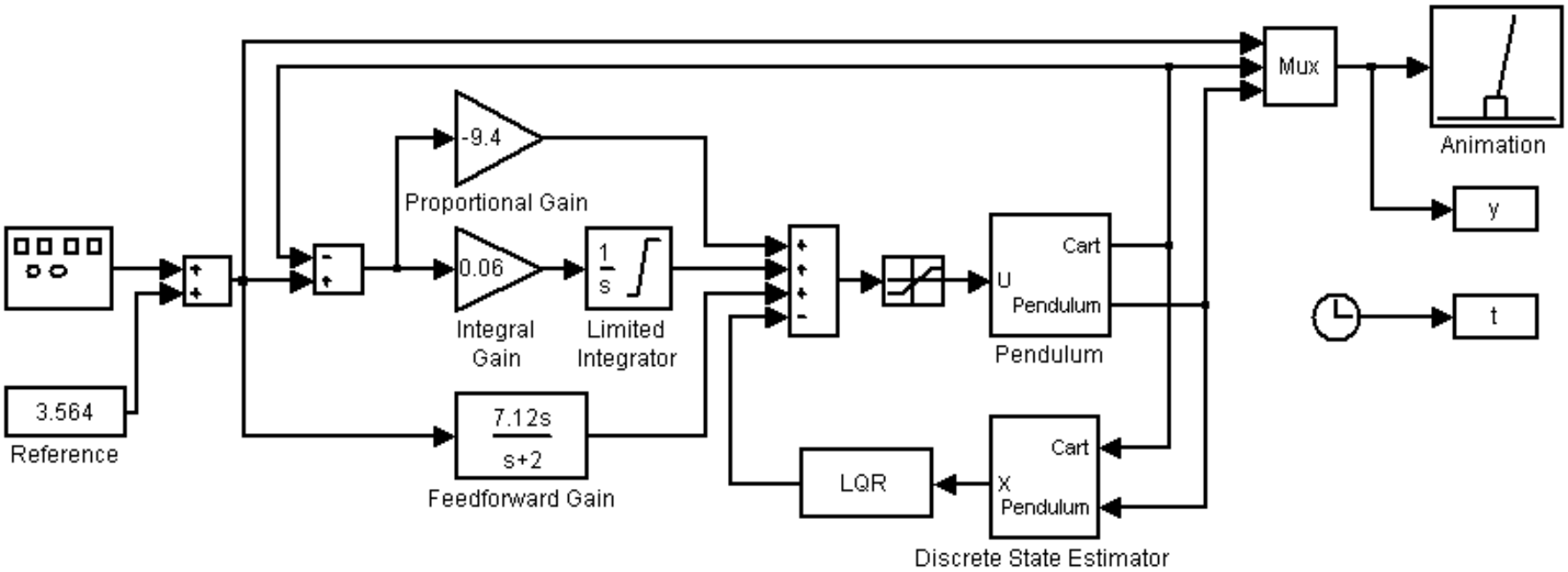
Layout Gallery (1/5): Original Layout



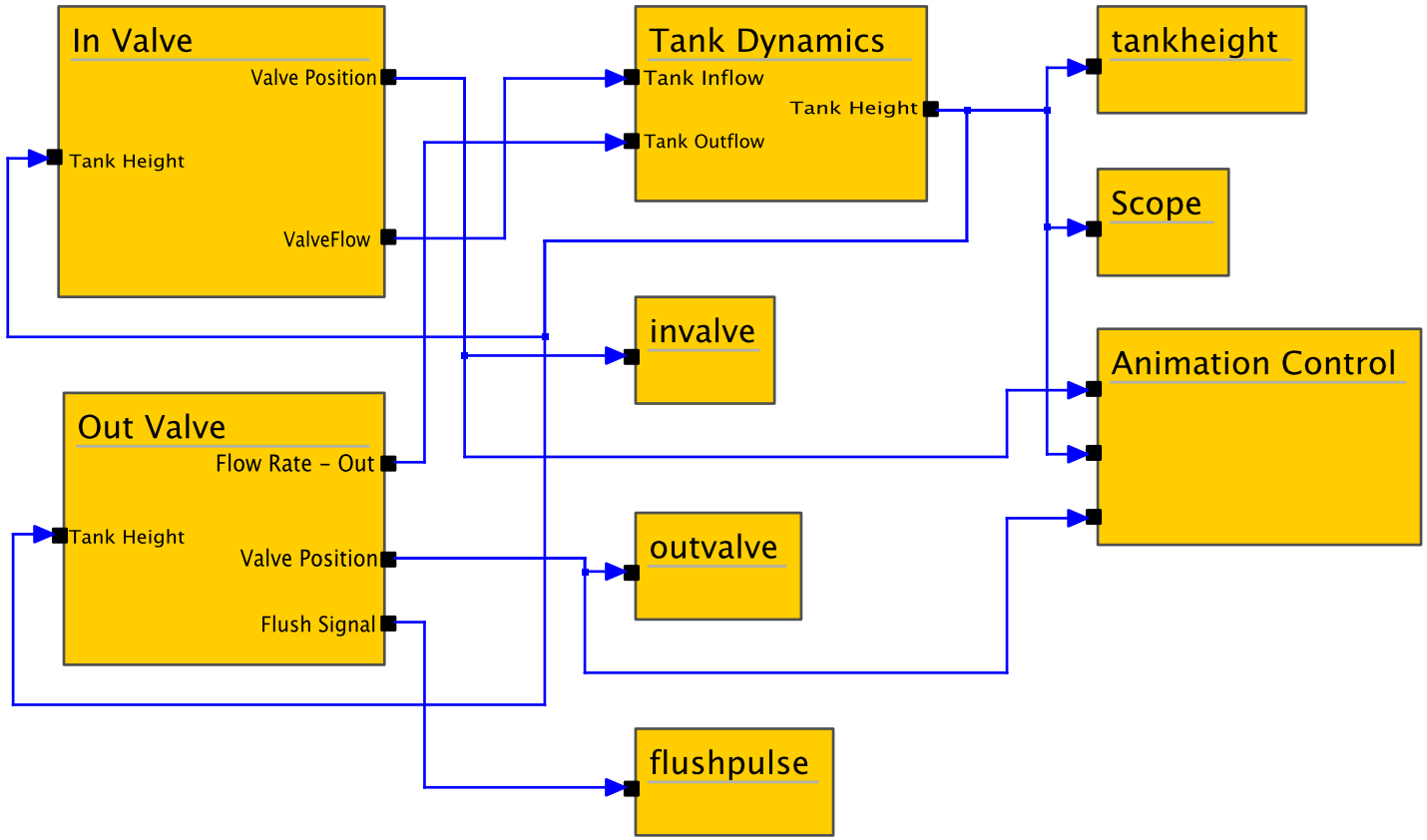
Layout Gallery (2/5)



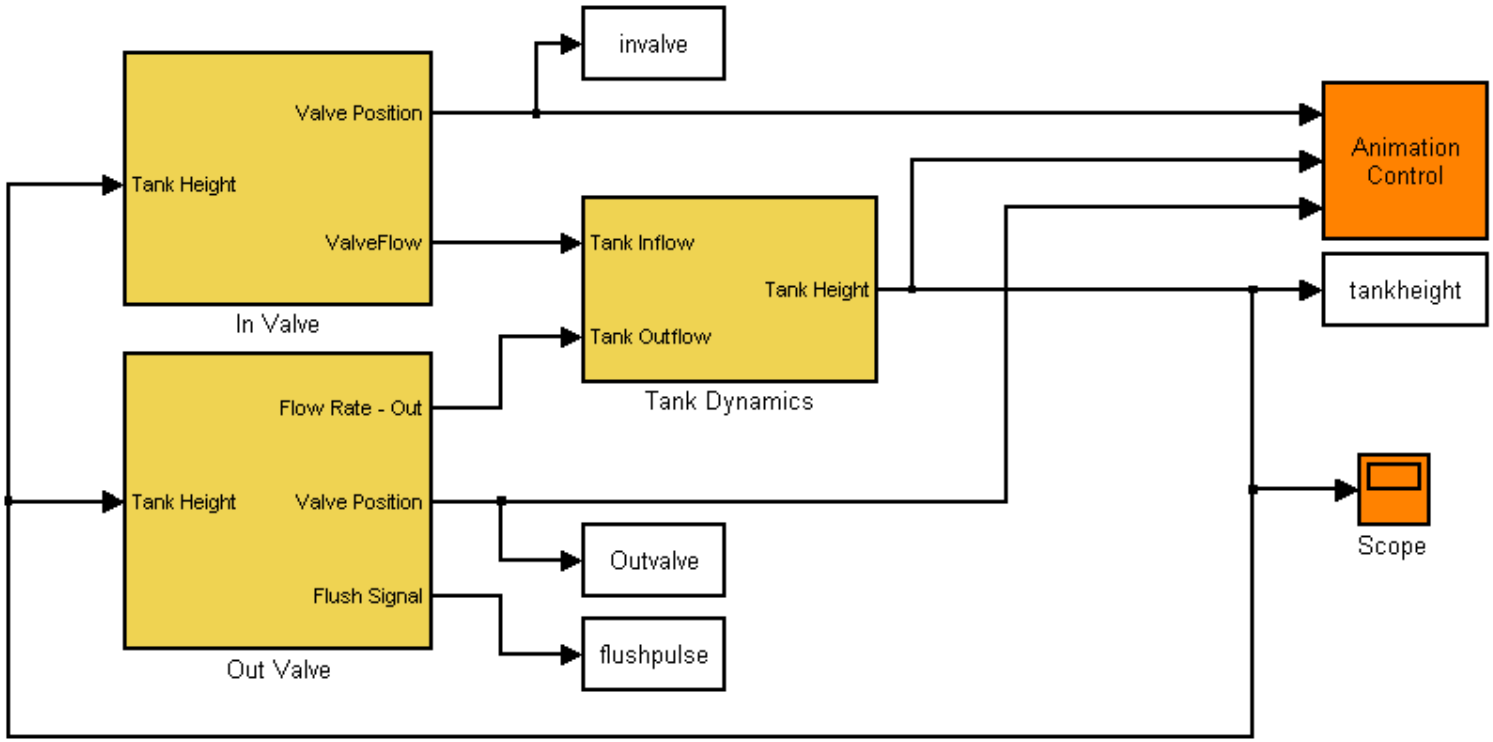
Layout Gallery (2/5): Original Layout



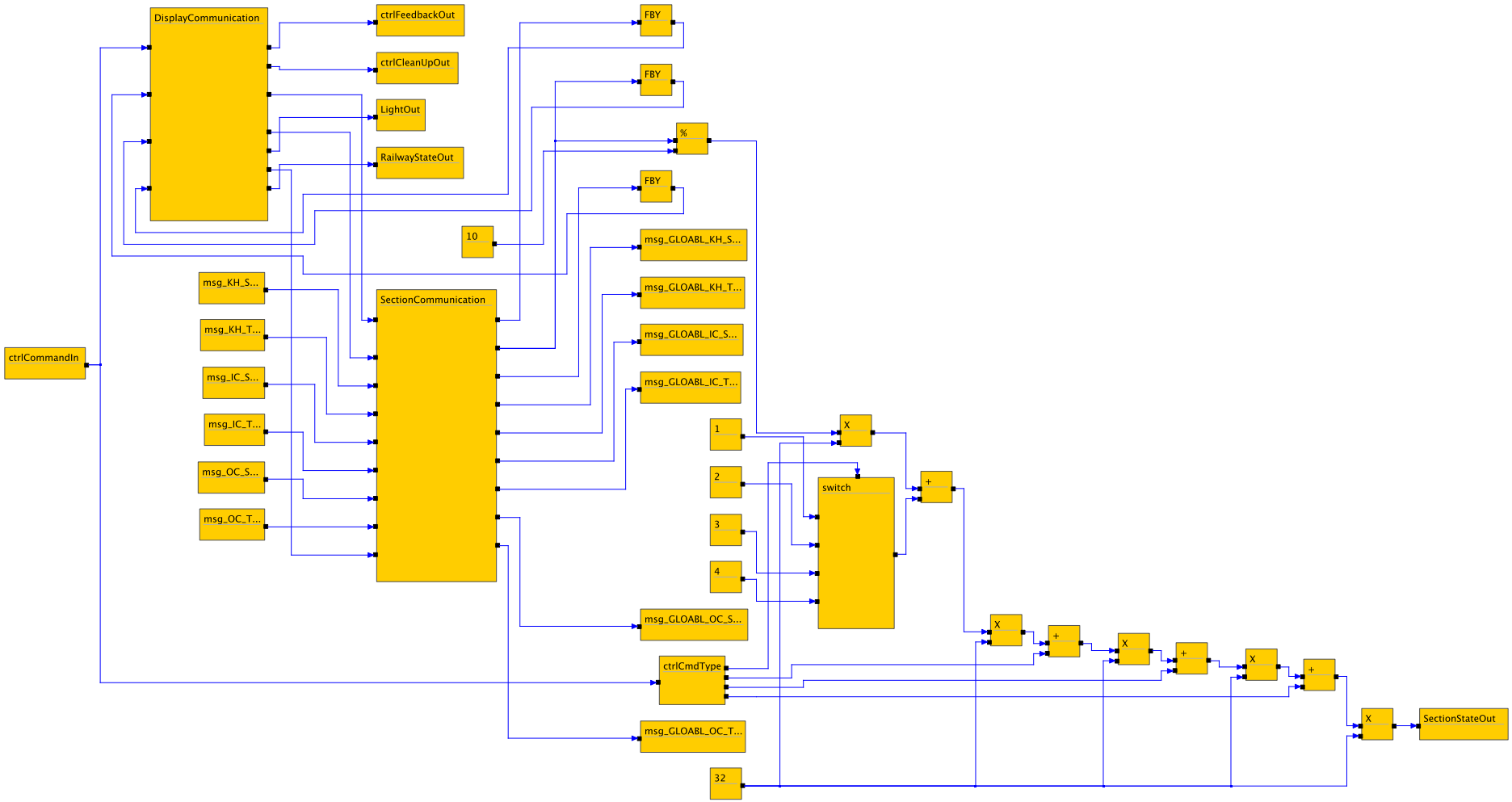
Layout Gallery (3/5)



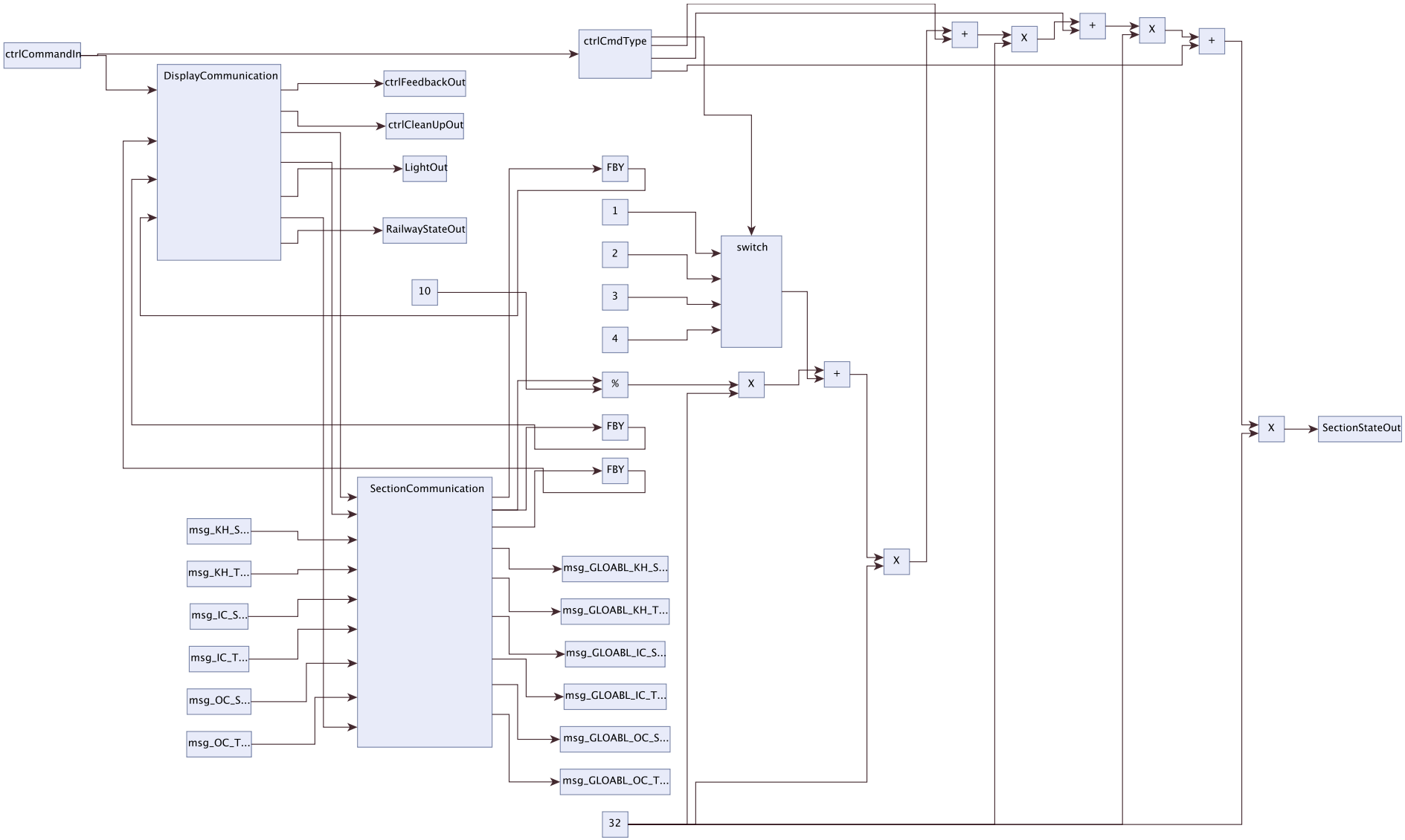
Layout Gallery (3/5): Original Layout



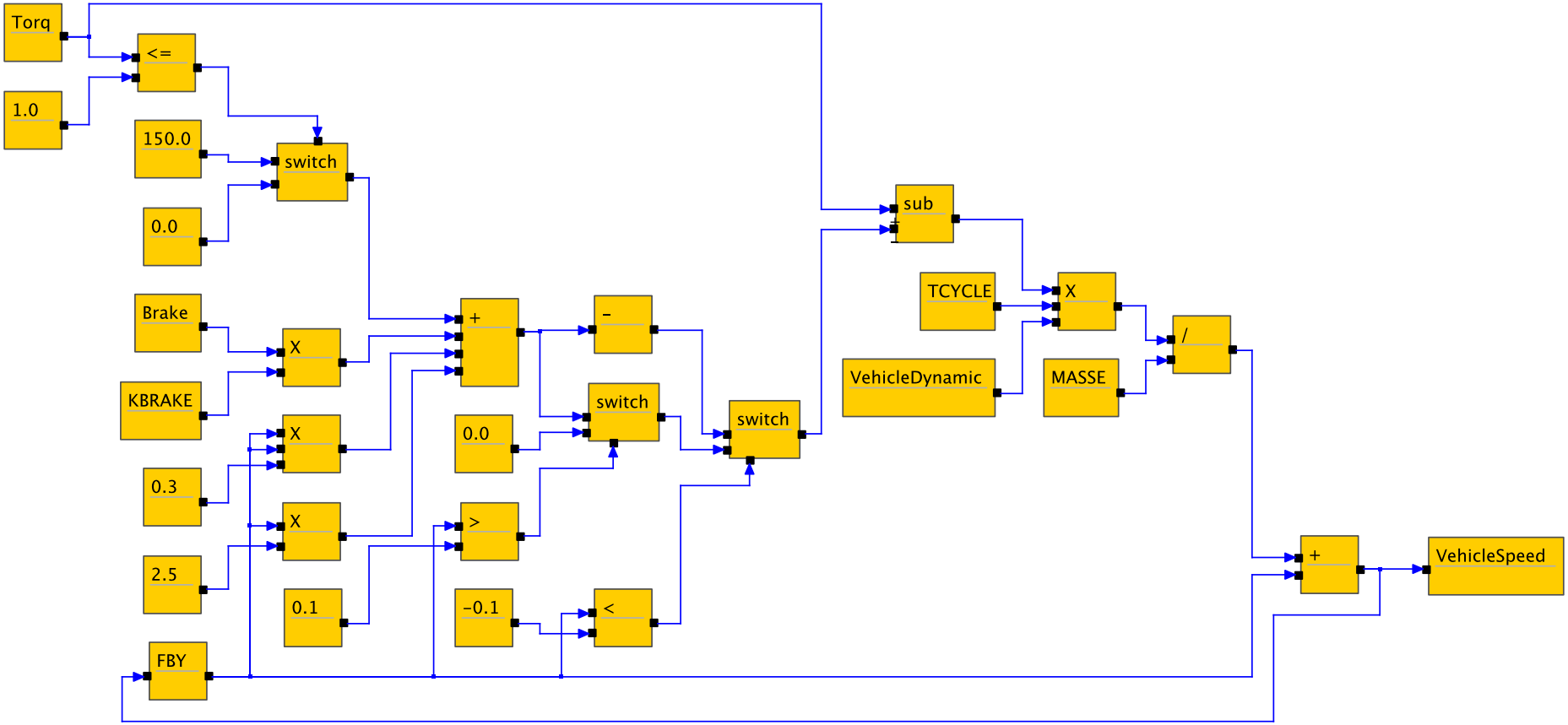
Layout Gallery (4/5)



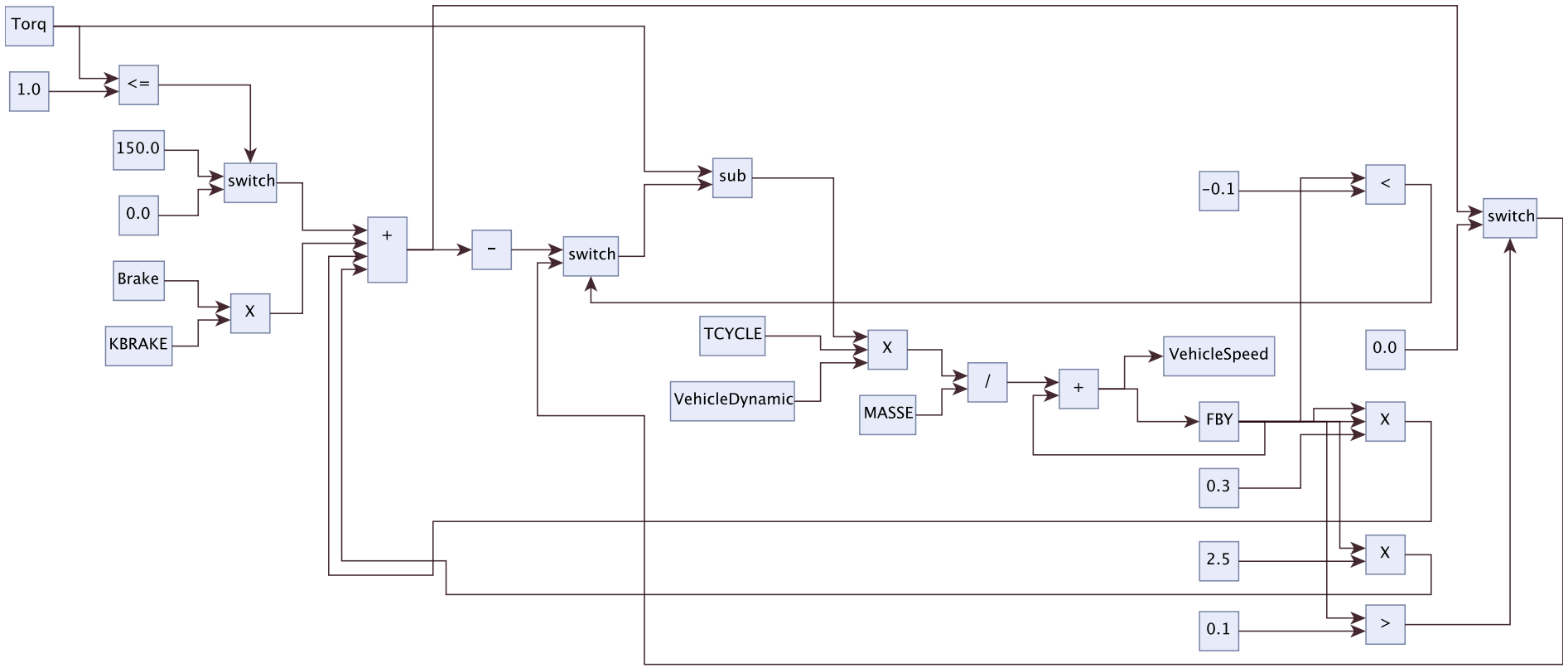
Layout Gallery (4/5): yFiles Layout



Layout Gallery (5/5)

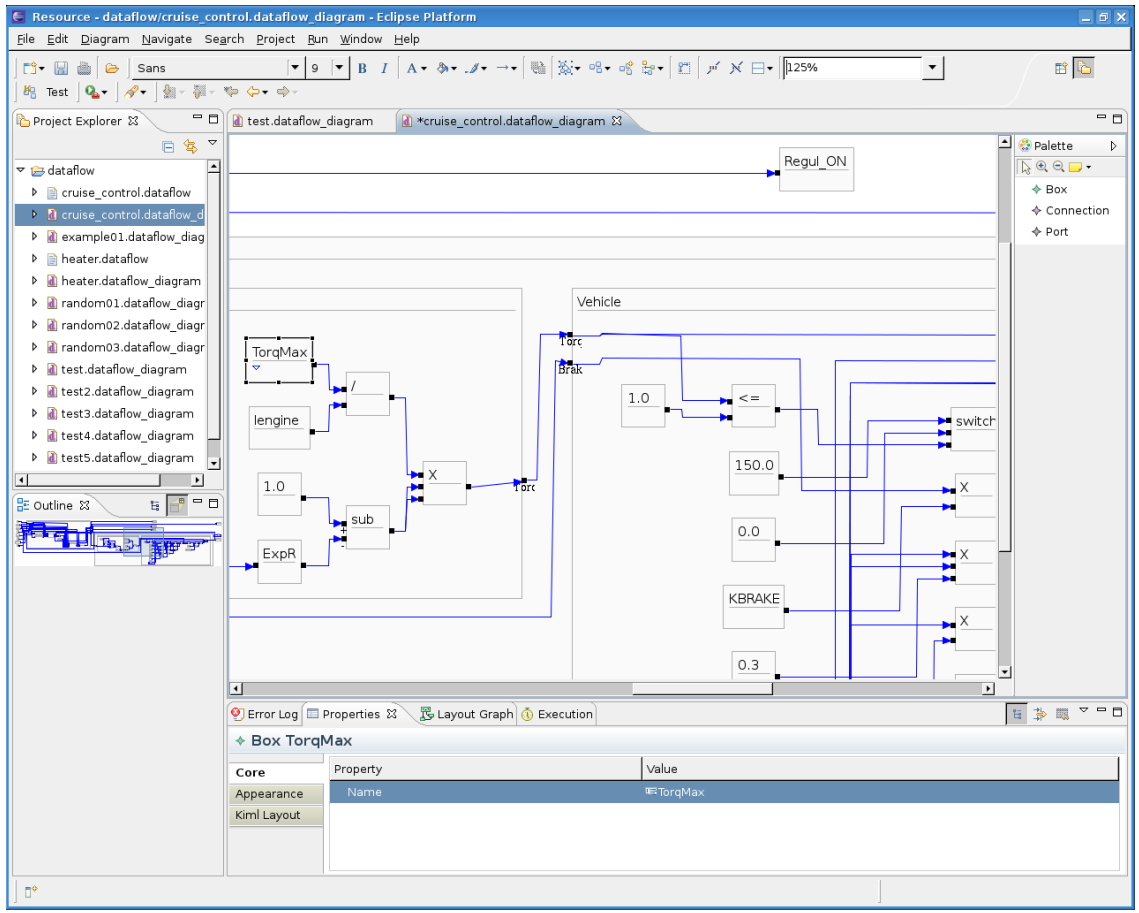


Layout Gallery (5/5): yFiles Layout



Application: KIELER

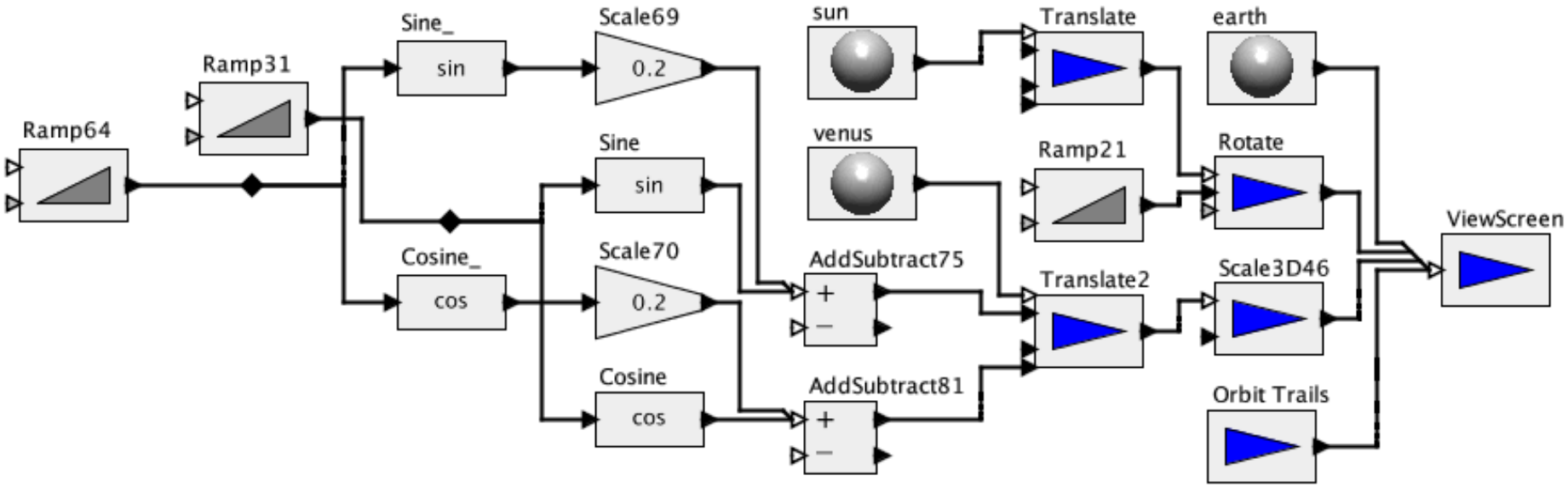
- Research project on graphical modeling, built on Eclipse
- Platform for development of layout algorithms for graphical modeling, open source



www.informatik.uni-kiel.de/rtsys/kieler

Application: Ptolemy

- Research project on concurrent real-time systems (UC Berkeley)



`ptolemy.eecs.berkeley.edu`

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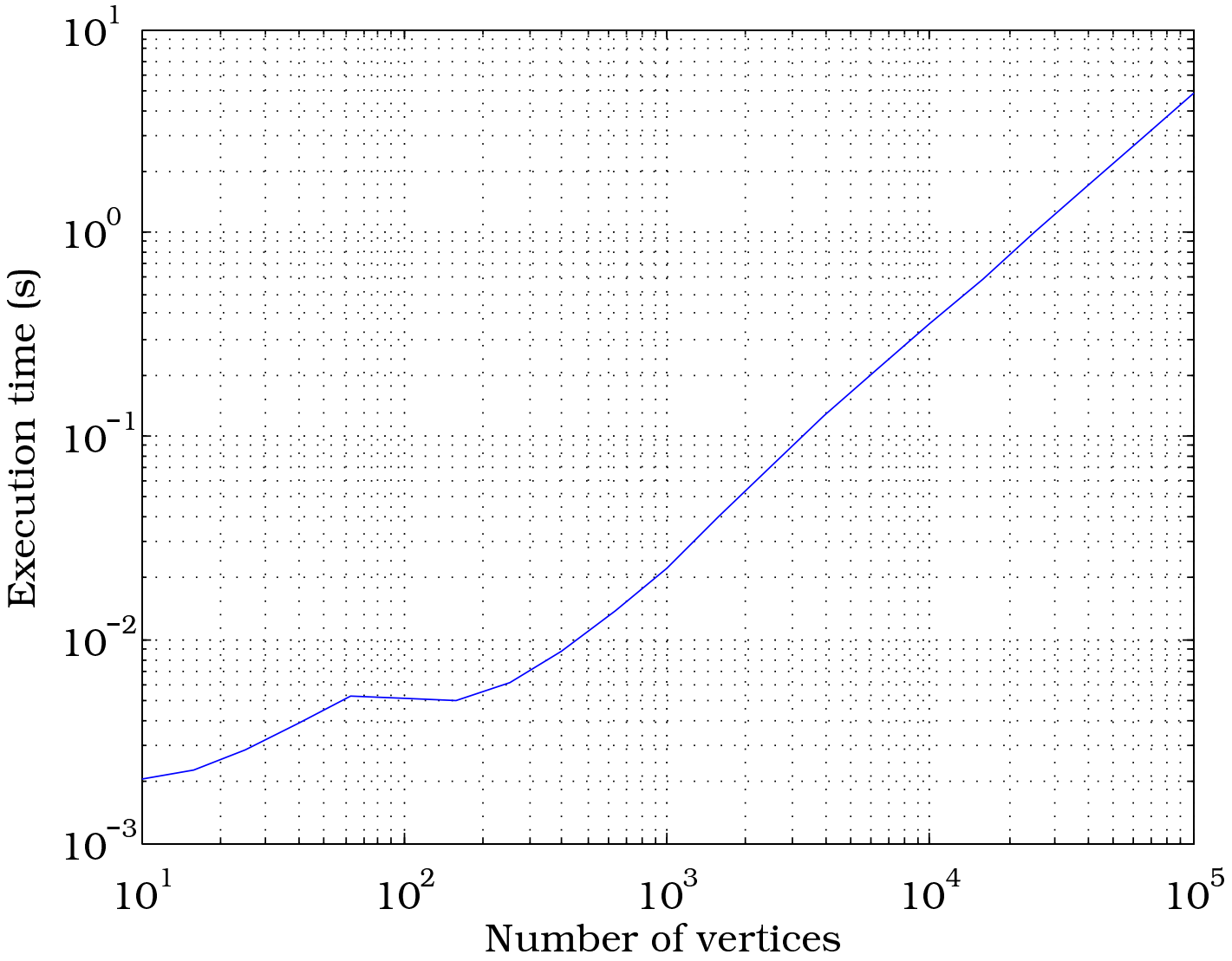
Thanks for your attention

`www.informatik.uni-kiel.de/rtsys/kieler`

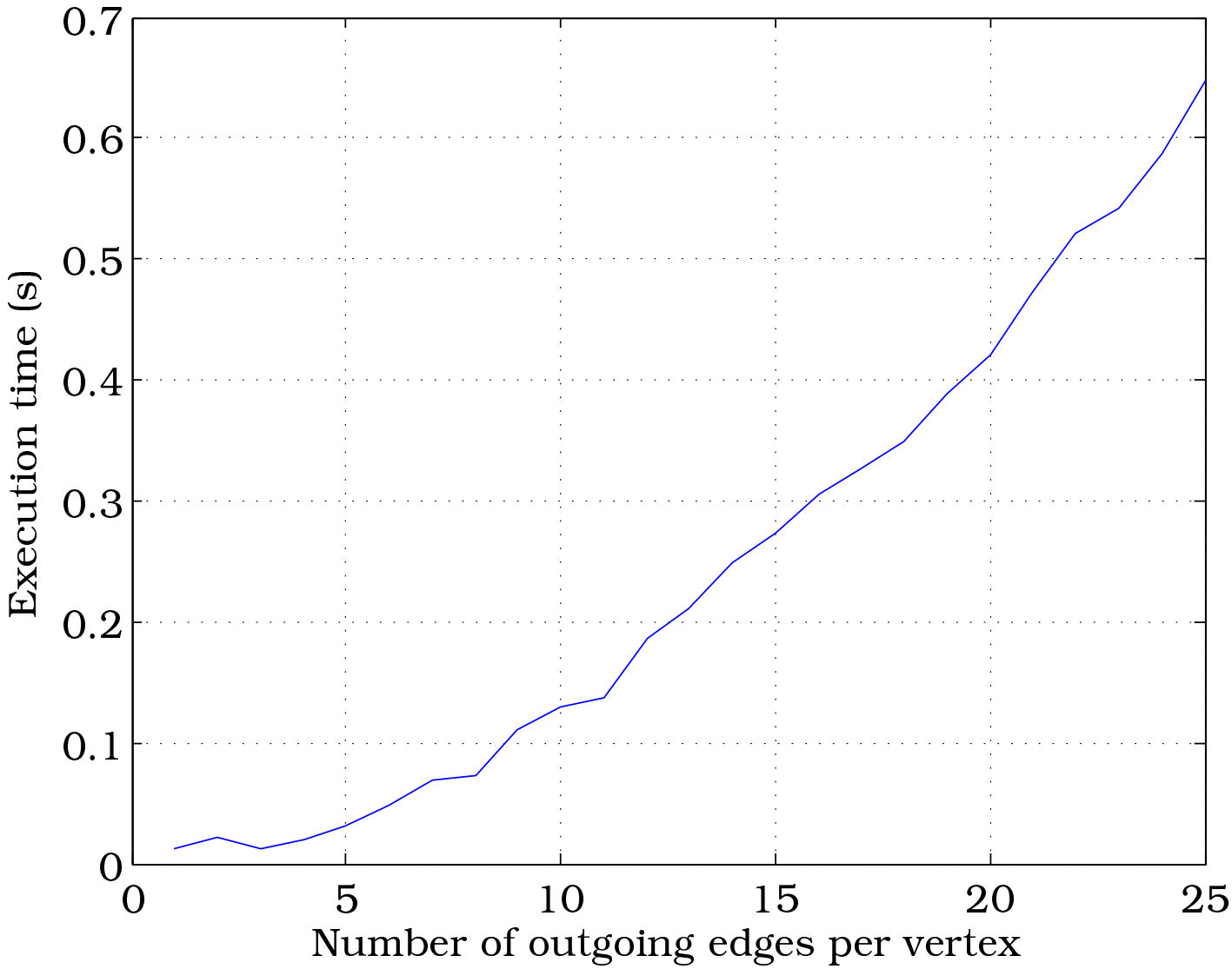
Appendix: Execution Time

Varying number of vertices, one outgoing edge per vertex

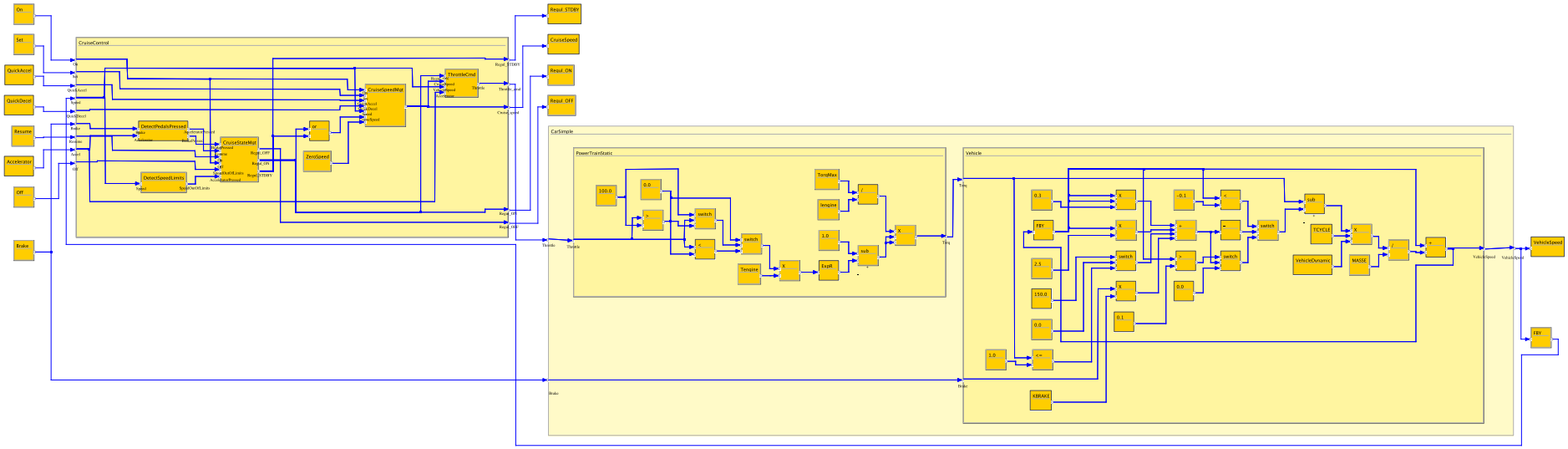


Appendix: Execution Time

100 vertices, varying number of outgoing edges per vertex



Appendix: Compound Diagram Layout



Appendix: Random Diagram Layout