# Improved Layout for Data Flow Diagrams with Port Constraints

Lars Kristian Klauske<sup>2</sup> Miro Spönemann<sup>1</sup> Christoph Daniel Schulze<sup>1</sup> Reinhard von Hanxleden<sup>1</sup>



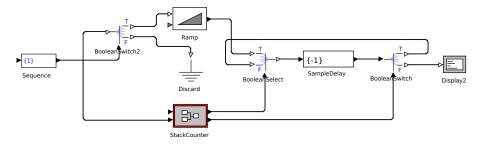
<sup>1</sup>Real-Time Systems and Embedded Systems Group Department of Computer Science Christian-Albrechts-Universität zu Kiel

<sup>2</sup>Daimler Center for Automotive Information Technology Innovations, Berlin

July 3rd / Diagrams 2012

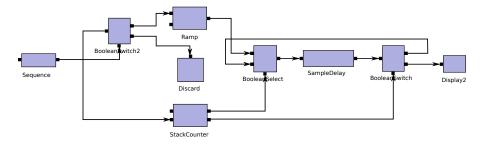
## Port-Based Data Flow Diagrams

A Ptolemy Actor Diagram (Edward A. Lee, UC Berkeley)



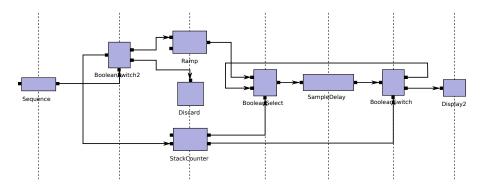
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## Outline

#### The Importance of Port Support Preliminaries Inverted Ports

Side Ports Putting It All Together

#### 2 Demo Time!

#### 3 Evaluation

#### **4** Conclusion

## Outline

# The Importance of Port Support Preliminaries

Inverted Ports Side Ports Putting It All Together

#### 2 Demo Time!

#### 3 Evaluation

#### Occursion

## Layer-Based Layout Algorithms

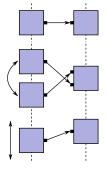
Based on Sugiyama et al. (1981)

Five phases:

2 Layer assignment

3 Crossing reduction

4 Node placement



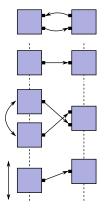
# Layer-Based Layout Algorithms

Based on Sugiyama et al. (1981)

#### Five phases:

- Cycle removal
- 2 Layer assignment
- 3 Crossing reduction

4 Node placement



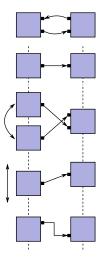
# Layer-Based Layout Algorithms

Based on Sugiyama et al. (1981)

#### Five phases:

- Cycle removal
- 2 Layer assignment
- 3 Crossing reduction

- 4 Node placement
- 6 Edge routing



Based on Spönemann, Fuhrmann, von Hanxleden, Mutzel (2009)

Five levels of freedom:

1 Free



Based on Spönemann, Fuhrmann, von Hanxleden, Mutzel (2009)

Five levels of freedom:

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2 Fixed Sides





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8 Fixed Order

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3 Fixed Order

4 Fixed Ratio









Based on Spönemann, Fuhrmann, von Hanxleden, Mutzel (2009)

Five levels of freedom:

Free

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3 Fixed Order

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#### 6 Fixed Positions











#### **Related Work on Port-Based Diagrams**

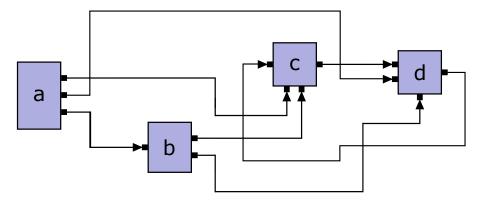
A Selection of Publications

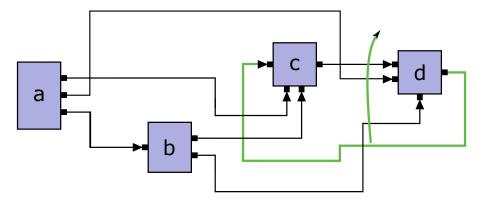
- Gansner, Koutsofios, North, Vo (1993)
  - Ports considered during node placement, not crossing reduction
- Sander (1994)
  - Routing of side port edges encapsulated in single dummy node
- Waddle (2001)
  - Considers order of ports during crossing reduction
- Spönemann, Fuhrmann, von Hanxleden, Mutzel (2009)
  - Introduction of port constraints and a basic layout algorithm
- Klauske, Dziobek (2010, 2011)
  - Port positions depend on (modifiable) node size

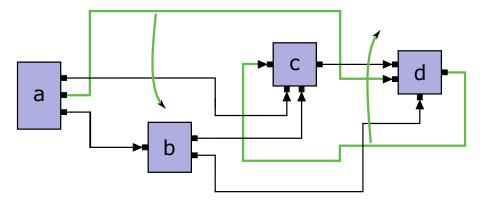
### Related Work on Port-Based Diagrams

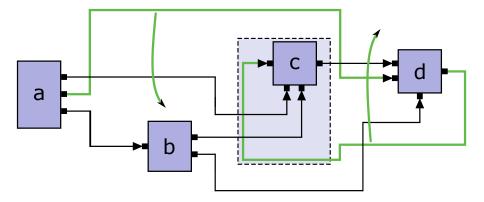
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  - Port positions depend on (modifiable) node size
- Wybrow, Marriott, Stuckey (2012)
  - More targeted towards network diagrams
  - However, application to data flow diagrams could be interesting



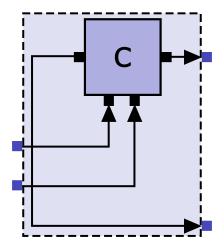






#### The Problem: Node-Local Edge Routing

Making Strange Nodes Look Perfectly Ordinary



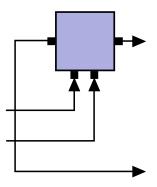
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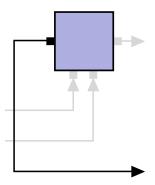
 The Importance of Port Support Preliminaries
Inverted Ports
Side Ports
Putting It All Together

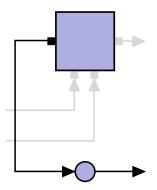
#### 2 Demo Time!

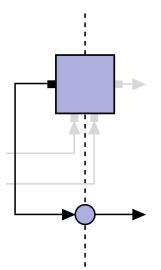
3 Evaluation

4 Conclusion









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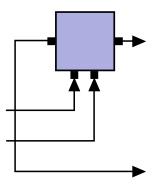
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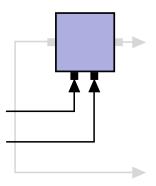
Preliminaries Inverted Ports Side Ports Putting It All Together

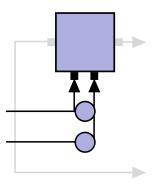
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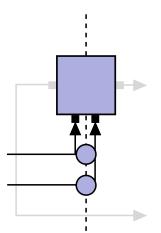
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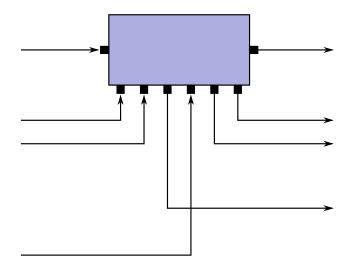
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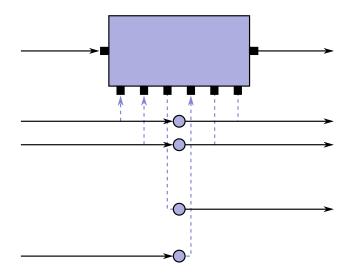


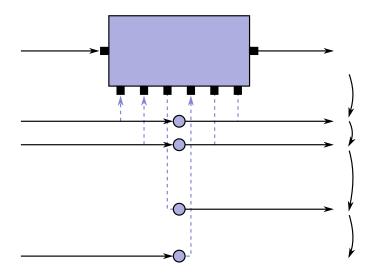


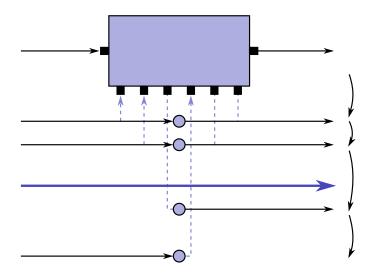






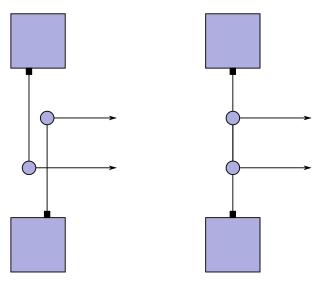






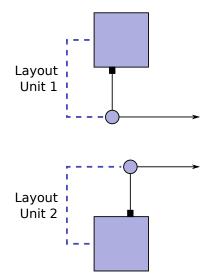
## Getting the Order of Dummy Nodes Right

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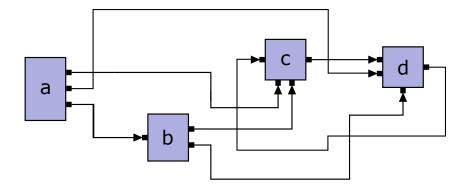
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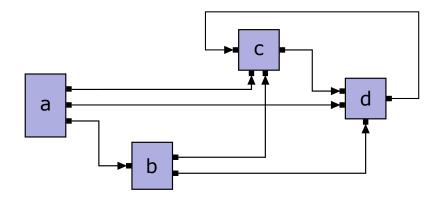
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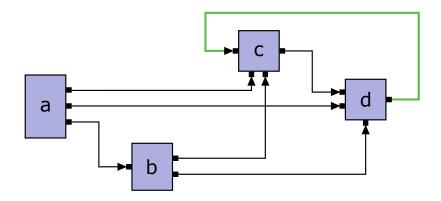
Layout Produced by Our Previous Algorithm



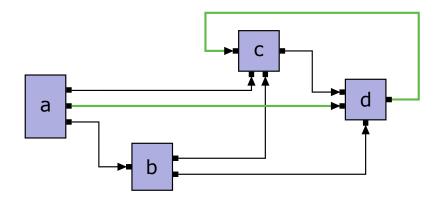
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#### B Evaluation

### 4 Conclusion

## See the Algorithm in Action!

Please stand by for the KIELER tool to appear...



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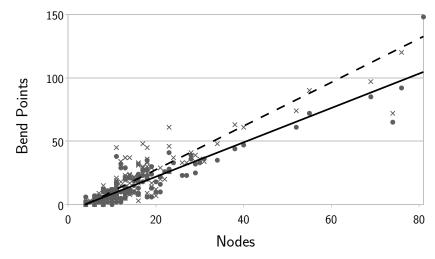
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# Layout Quality (Ptolemy Diagrams)

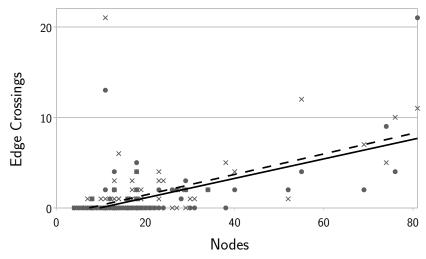
Current Algorithm (solid) vs. Previous Algorithm (dashed)



141 Ptolemy demo models, up to 43 nodes per hierarchy level (avg. 8.98)

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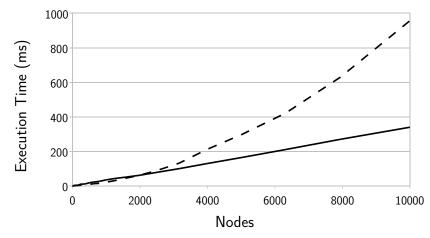
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### **Runtime Performance**

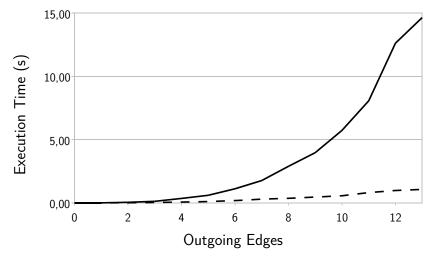
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Random graphs with 10 to 10,000 nodes, 0 to 2 outgoing edges each

### **Runtime Performance**

Current Algorithm (solid) vs. Previous Algorithm (dashed)



Random graphs with 100 nodes, fixed number of outgoing edges

## Outline

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What Did Just Happen?

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- Examples of what still remains to be done:
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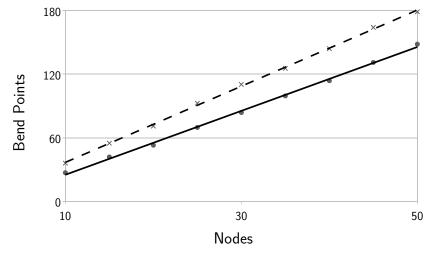
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Feel free to pay us a visit and look at our KIELER platform at www.informatik.uni-kiel.de/rtsys

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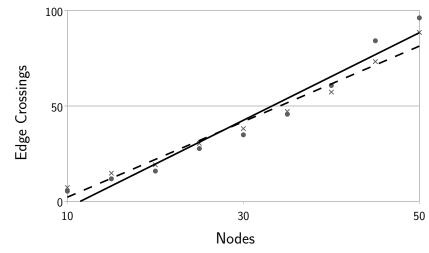
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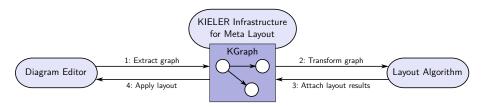
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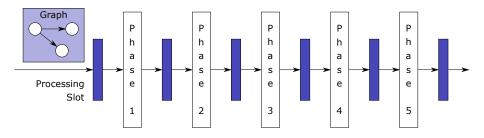
## **Connecting Editors and Layout Algorithms**

The KIELER Infrastructure for Meta Layout



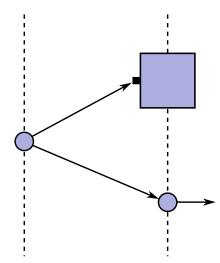
## The Algorithm's Architecture

Interchangeable Phases and Intermediate Processors



### **Inverted Ports**

A Solution with Two Dummy Nodes



## Basic Support for Node and Port Labels

Reserving Space through Bounding Boxes

